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DESIGN, TESTING, AND EVALUATION OF GaAs PN SEQUENCE GENERATOR CIRCUITS IMPLEMENTED IN DCFL AND TDFL

By

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September 1997

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Spaceborne and military communications hardware demands very high speed circuitry even under high radiation exposure. GaAs field effect transistors have the desirable quality that they possess rapid switching rates and are inherently more resistant to total-dose radiation induced failure than their silicon CMOS counterparts. This thesis project involves the design, simulation, submission for fabrication, testing, and evaluation of a 1-GHz, 7-bit, pseudo-noise sequence generator (PNSG) which has numerous communications applications, particularly in spread-spectrum communications. The basic design of the PNSG is provided first, then topology-specific design considerations are covered for directly-coupled FET logic (DCFL) and two-phase dynamic FET logic (TDFL) implementations. Analysis and comparison of circuit performance characteristics are completed, demonstrating the significant improvements in speed, layout area, and power consumption that dynamic logic offers.

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I. INTRODUCTION

As society's dependence on technology-based solutions increases at a growing rate, the demand for very high speed digital processing and communications equipment grows commensurately. Gallium arsenide (GaAs) semiconductor-based chips offer substantial speed improvement over their silicon counterparts. Satellite-borne digital hardware has the additional demand that it be radiation hardened because of the hostile radiation environment of space. Here, too, GaAs offers an inherent advantage as it possesses a higher tolerance to total-dose radiation effects than comparable silicon-based hardware.

Spread spectrum communications systems employ pseudo-random or pseudo-noise sequences extensively for purposes of synchronization and encoding. These systems would be served well by improvements in the speed, power consumption, and radiation tolerance of the pseudo-noise sequence generators (PNSG) they utilize. Such improvements are available through the use of GaAs integrated circuits.

This thesis addresses the issue of GaAs circuit design, layout, and characterization through the implementation of a 7-bit PNSG. Of primary focus are the differences between static and dynamic logic topologies, particularly the power savings afforded by the dynamic logic implementation. Chapter II will provide background information concerning GaAs characteristics and GaAs FETs. Chapter III reviews the basics of the PNSG and Chapters IV and V cover the design and testing of the static and dynamic implementations respectively.

II. BACKGROUND

A. HISTORICAL REVIEW OF GaAs ICs

GaAs is a III-V compound semiconductor, meaning its elemental components gallium and arsenic are found in columns III and V of the Periodic Table of Elements. It has been used as a semiconductor since the 1960's; the first diffusion gate structure GaAs transistor was fabricated in 1967 with a frequency range in the low MHz. By 1971 the technology had matured to the point where a 1 μm gate length FET could be created with useable gain up to 18 GHz. Initial uses of GaAs focused on circuits requiring strong high frequency performance or that took advantage of optical properties of GaAs; these included microwave amplifiers and opto-electronic devices such as light-emitting diodes (LEDs), laser diodes, and optical sensors. Digital uses have followed with the first small scale GaAs ICs being produced in the early 1970's. The rapid switching time characteristic of GaAs FETs has made their use particularly attractive to efforts demanding high-speed circuitry. While the scale of integration in GaAs ICs has lagged behind that of silicon complementary metal-oxide-semiconductor (CMOS) FETs, numerous large scale ICs (LSI) components have been produced in GaAs and some very large scale IC (VLSI) components have been demonstrated. Contributing to this developmental lag has been the difficulty in obtaining low defect density materials required for high yield processes. Additionally, the inability to develop p-Schottky barrier junctions has prevented the realization of p-channel MESFETs (metal semiconductor field effect transistor). Some progress has been made in developing

complementary GaAs processes but much of the GaAs design still makes exclusive use of n-mode GaAs FETs.[1,4]

B. CHARACTERISTICS OF GaAs

As with any technology, GaAs offers both advantages and disadvantages to the digital circuit designer. The primary benefits of using GaAs are its superior power-delay product and its inherent total dose and dose rate radiation hardness. Some of the challenges inherent in GaAs use include greater difficulty in creating complementary logic FETs, higher fabrication costs, and heat dissipation problems. In this section, the characteristics of GaAs are briefly examined.

1. Carrier Mobility

The speed advantage that GaAs enjoys over Si is due primarily to the significantly higher electron mobilities. Carrier mobility is defined as the ratio of the carrier velocity to the electric field present and is expressed in units of $cm^2/V \cdot sec$. For low electric fields ($|E| < 4$ kV/cm), GaAs electron mobility is dramatically higher than that of Si, 5000 $cm^2/V \cdot sec$ as compared to 800 $cm^2/V \cdot sec$ at a donor concentration of $10^{17}/cm^3$. This high electron mobility translates into higher transconductance and thus, dramatically faster switching times for the FET. A more revealing parameter of a logic technology is its power-delay product which provides a clearer sense for how much power must be expended to achieve a desired circuit speed. The power-delay product of a logic gate is calculated by taking the product of the gate delay by the average power consumed by the

gate. When comparing equivalent size circuits, GaAs enjoys an approximate five-fold advantage over silicon in power-delay product. [1, 4]

The electron mobility of GaAs is impressive in comparison to Si but the hole mobility is not. A typical low-field hole mobility for p-type GaAs is on the order of 250 $cm^2/V \cdot sec$ compared to about 300 $cm^2/V \cdot sec$ for p-type Si. GaAs shows more than an order of magnitude difference between its electron and hole mobilities. The inability to fabricate p-channel MESFETs has been a primary factor in the difficulty of creating commercially viable complementary logic using GaAs MESFETs. [1]

2. GaAs: a Semi-Insulator

Another characteristic of GaAs is that its intrinsic resistivity is considerably higher than that of silicon. The higher intrinsic carrier density of silicon demands the use of isolation to prevent leakage between devices. P/N junctions are used which result in higher parasitic capacitances. GaAs is largely spared the necessity of doped wells due to its higher resistivity, thus parasitic capacitances are reduced. This further increases the high frequency performance of GaAs FETs. [1]

While the substrate has a higher natural resistivity, efforts to create a thin, effective oxide layer for insulating gate junctions have not been particularly successful. For this reason, a GaAs metal-oxide-semiconductor has not become available for production. Instead, the use of a Schottky metal layer directly on top of the channel is the fabrication standard for GaAs. This configuration is referred to as a metal-semiconductor FET or MESFET. The disadvantage of the MESFET is that current can flow through the

gate electrode to the source. This gate-source conduction effectively clamps the input high voltage of a GaAs MESFET to the threshold voltage of the Schottky barrier diode which forms at the metal-semiconductor junction; the Schottky diode typically has a threshold voltage of 0.6 to 0.7 V. Pinchoff voltages are limited by this effect and FET threshold voltages must be kept well below these values. This forces noise margins for GaAs to be in the range of 100-250 mV. Figure 1 shows the basic difference in design between a GaAs MESFET and a Si MOSFET.

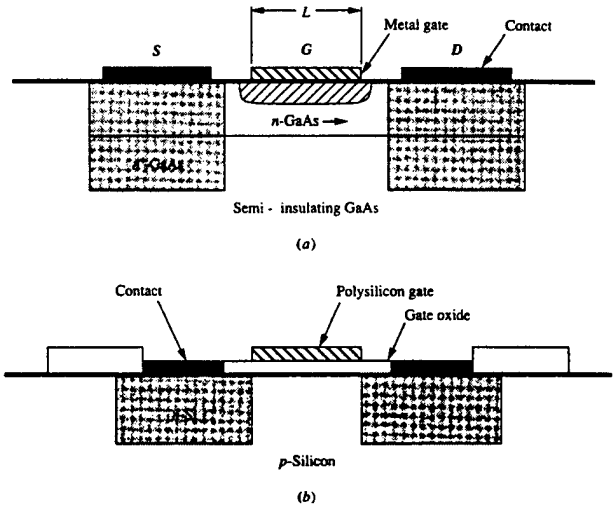


Figure 1 Cross-section of (a) MESFET and (b) MOSFET from Ref. [1].

3. Radiation Hardness

GaAs enjoys an inherently higher total-dose radiation immunity than its silicon counterpart. Because GaAs MESFETs do not utilize a gate oxide which changes charge state when exposed to ionizing radiation, GaAs MESFETs are immune to total ionizing dose effects. The surface of the GaAs substrate contains a high density of energy states

which act to absorb charge. This charge collection behavior is the key to GaAs radiation hardness because radiation produces stray currents (moving charges) which have the potential of upsetting the proper behavior of the transistor. The long-term benefit of surface absorption in GaAs is that device parameters (V_T and parasitic resistance) remain fixed and large surface currents are suppressed to a much greater extent than in Si.

Radiation effects are typically broken into three main categories: total-dose effects, dose-rate effects, and single event effects (SEE). GaAs is less susceptible to dose-rate effects due to its higher inherent resistivity. The two most important SEEs are single event induced latchup and single event upsets (SEUs). Because GaAs makes no use of well structures, the former can not occur in GaAs circuits. SEUs can occur as a result of a single cosmic particle inducing photo-currents in the depleted channel of the MESFET. GaAs has a wider band gap energy than Si and thus tends to be less sensitive to transient radiation effects, provided the GaAs substrate is undoped and of high quality. [2, 7]

4. Thermal Conductivity

GaAs has a lower thermal conductivity that Si. This means that for equal power consumption, the GaAs chip will run hotter as it is unable to deliver the heat away from the inner chip as quickly. This, in turn, leads to higher thermal gradients across the GaAs chip. This characteristic means that when designing LSI and VLSI GaAs chips, heat dissipation issues are more critical than with Si semiconductors.

5. Fabrication Cost

The lower noise margins of GaAs result in reduced yields for VLSI chips in comparison to Si chips of comparable complexity. Also, GaAs crystal growth is less mature than that of Si so that GaAs wafers are generally smaller and of poorer quality resulting in fewer functional chips per wafer. These effects add up to higher cost per functional chip. [4] Historically, this higher cost has meant that GaAs was viewed as a more exotic solution, used only when cost was secondary in importance to speed and radiation hardness. Military and space-based applications were some of the first to take advantage of GaAs digital circuitry. In the last three years, substantial progress has been made in MESFET technology such that its commercial use has grown significantly.

C. N-TYPE AND P-TYPE MESFET'S

When a semiconductor material such as GaAs is undoped, it generally has a fairly high resistivity. In the case of GaAs, this resistivity is typically on the order of 10^6 to 10^8 Ω·cm [1]. As was stated in the last chapter, GaAs is often referred to as semi-insulating rather than semi-conducting. When a dopant is added to the semiconductor, a surplus or deficit of conducting electrons is established. If the doping creates a surplus of electrons, such as is the case when phosphorous is the dopant, this state is referred to as an n-type material because the electrons carry a negative charge. Conversely, a dopant that creates a deficit of conducting electrons, beryllium for example, forms a p-type material because a shortage of electrons, or holes as they are known, have a positive charge. As previously mentioned, p-channel transistors in GaAs have a much lower

carrier mobility than n-type, as much as 20 times lower. This disparity makes complementary MESFETs more challenging to produce. This thesis project, therefore, makes exclusive use of n-type GaAs FETs.

D. E-MODE AND D-MODE MESFET'S

While the FETs of this thesis will rely on electrons as the carrier, that is n-type FETs, it is possible to adjust the threshold voltage, V_T, of a transistor such that it either conducts or does not conduct when the gate-source voltage, V_{GS}, is at zero volts.

1. Depletion-mode FET

If the threshold voltage, V_T, is less than 0V, then the FET is said to be a depletion-mode FET (DFET). The transistor is said to be "ON" when the gate-to-source voltage,V_{GS}, is greater than the threshold voltage, V_T. A typical value of V_T for a DFET is around –0.85V. By increasing the donor concentration immediately below the gate, the transistor will conduct with zero voltage applied to the gate; a typical DFET doping concentration at the surface is 1E18/cm^3. Only if a sufficiently strong negative voltage is applied to the gate will the electron carriers be displaced to a lower position rendering the transistor effectively non-conducting, or "off." When DFETs are used, V_{DS} is normally kept at a positive level throughout the operating range of the circuit. Circuits that use DFETs exclusively have the problem of unequal input/output logic levels. This requires added circuitry, additional power supply rails, and generally greater power consumption. The primary advantage of DFET-only circuits is that the voltage swings between logic

levels can be larger which increases noise margins. [4] This thesis, however, makes use of E/D MESFETs which use DFETs for pull-up to V_{dd} and EFETs for switching to ground.

2. Enhancement-mode FET

If V_T is great than 0V, then the FET is considered an enhancement-mode FET (EFET). In the case of EFETs, the channel below the gate is not as heavily doped as with DFETs such that with no voltage applied to the gate, the channel is effectively non-conducting. The surface doping concentration for an EFET is normally in the range of 5E17/cm^3. When a positive voltage of ample magnitude is applied to the gate, however, electron carriers are drawn into the channel producing a conducting path between the source and drain. This threshold voltage, V_T, of the GaAs EFET is nominally 0.25V. EFETs have the characteristic that above a certain gate-source voltage, V_{GS}, current flows from gate to source. This gate conduction is a Schottky barrier diode and typically is forward biased at around 0.7V. Consequently, with EFETs the voltage swing between logic levels is limited by the forward gate-source conduction. This smaller voltage range for V_{GS} combined with the low V_T demands that the threshold voltage be tightly controlled and very uniform, both within a chip and between chips. Deviations in V_T introduce possible logic errors and thus reduce yield. Additionally, the smaller voltage swing translates into reduced noise margins.

E. STATIC LOGIC

1. Basic Description

A logic topology which does not rely on any clocking and where the output depends only on the input values propagating through the circuitry is said to be static. One type of static logic is called ratioed-logic because the speed, power, high and low voltages, and noise margins depend heavily on the ratio of the lengths and widths of the FETs used. In ratioed static logic, static power is dissipated which is to say that current is flowing (by design) from supply to ground while the gate is at a particular logic state. There are several common static logic topologies in GaAs, including directly-coupled FET logic (DCFL), super-buffer FET logic (SBFL), source-coupled FET logic (SCFL), capacitor-coupled logic (CCL), and capacitor-diode FET logic (CDFL). The static implementation of the PNSG in this thesis was designed and fabricated using DCFL with superbuffers used as necessary when internal current demands warranted their use. DCFL will be discussed in more detail below.

2. Design Considerations

The design of GaAs static circuitry is complicated by the lack of standards, unlike Si where factors such as logic levels, supply voltages, and preferred topologies have a much higher degree of commonality in the industry. Further complicating GaAs static design is the variation of threshold voltage from one fabrication process to another. [1]

The most basic fabrication parameters over which the digital designer has control are the width and length of the gate. Generally, as gate width is increased, power and

speed go up because a wider gate can support a larger current. However, the layout area and gate capacitance are increased as well. Supply voltage can also be adjusted. When the supply voltage is reduced, power consumption generally follows but then voltage swings and current are also reduced resulting in lower noise margins and lower speed operation. It is up to the design engineer to determine what performance is required and what tradeoffs they are willing to make to obtain the desired circuit behavior in speed, power, layout area, yield and cost.

Static noise margins are determined primarily by the voltage gain of the circuit, the power supply voltage, and the symmetry of the transfer curve. Static noise margins generally describe how tolerant the gate output is to voltage swings at the input. It should be clear that circuitry which utilizes a smaller voltage swing will be very likely to have lower noise margins, neglecting effects due to asymmetry in the switching of the gate.

3. DCFL Topology

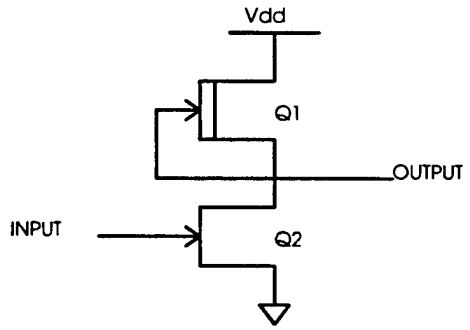


Figure 2 DCFL Inverter

Figure 2 depicts a basic DCFL inverter. Note that Q1, a DFET, is being used as a pull-up to V_{DD} and is often referred to as a "load" FET. Q2, an EFET, serves as the

switching transistor. It can be seen that the input voltage is limited by the gate-source conduction of the switching EFET to the threshold voltage of the Schottky barrier diode. While this reduced voltage swing tends to improve speed, noise margins suffer. In order to get a fairly symmetric transfer curve using the minimum gate length for the EFET and the minimum gate width for the DFET, the inverters used in this thesis contain EFET gates that are 16 μm in width and 0.8 μm in length and DFET gates that are 2.0 μm wide and 1.6 μm in length. In designing a DCFL GaAs circuit, it is important to insure that the output low voltage is safely below the threshold voltage of the EFET to provide for proper operation. Scaling the transistor widths and heights is the primary method of achieving this objective. Because of the negative impact on speed and noise margins that placing two EFETs in series has, the use of NAND gates was avoided entirely in this thesis, in both the DCFL and TDFL designs. Instead, NOR gates and inverters were utilized exclusively.

The advantage of the DCFL topology is its simplicity with few circuit elements per gate. This manifests itself in lower interconnect parasitics, greater gate density, reduced power consumption (compared to other high speed static logic circuits), and higher speed. [8] While DCFL does offer reasonable power per gate, it does have the disadvantage that when the output is low, the inverter is sinking current from V_{dd} to ground. That is to say, the DCFL topology consumes considerable static power when the output is low. It is this static power consumption which has motivated efforts to develop more power-frugal dynamic circuit topologies.

F. DYNAMIC LOGIC

1. Basic Description

Because of the difficulty involved in producing a viable complementary MESFET logic topology, static GaAs MESFET circuitry is subject to the substantial static power consumption described previously. Offering substantial reduction in static power consumption are logic topologies which rely on a clocking signal for their basic operation; such circuits are termed dynamic logic. The dramatic static power reduction is brought about by employing clocking to prevent a closed current path from existing between power and ground. Dynamic logic is often called non-ratioed-logic because circuit performance characteristics do not depend on the width and length ratios between FETs to the extent they do in static logic. This non-ratioed characteristic means that dynamic logic FETs can generally be made minimum size, thus requiring less layout area than a functionally equivalent static circuit. Various domino logic families and two-phase dynamic FET logic (TDFL) are the primary dynamic logic topologies in use with GaAs. The dynamic implementation of the PNSG in this thesis was designed and fabricated using the TDFL topology.

2. Theory of Operation

A dynamic circuit has two phases of operation, a precharge phase and an evaluate phase. Looking at the TDFL inverter in Figure 3, it can be seen that when $\Phi 1$ is asserted high and $\Phi 2$ is low the output of the inverter will be charged high through Q2; this is the precharge phase and the output is always high during precharge. When $\Phi 1$ goes low and

Φ2 goes high, the output will either discharge to ground through Q3 and Q4 or float high depending on the input voltage controlling Q4; this is the evaluate phase. This precharge-evaluate cycle is the essence of dynamic logic and it should be clear that the same transistors which regulate the precharging and evaluation are simultaneously preventing a completed path from supply to ground from forming.

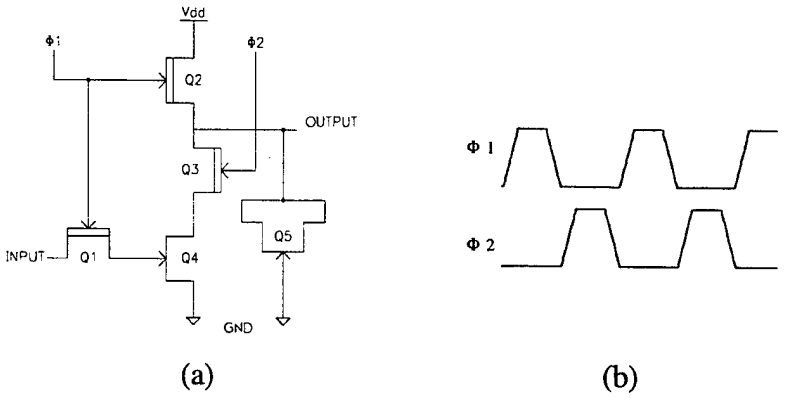


Figure 3 (a) TDFL Inverter and (b) Non-Overlapping Clocks, Φ1 and Φ2

As was stated, dynamic logic offers dramatic savings in power and more modest improvements in layout area, but at what cost? The principal costs of dynamic logic are increased routing since every dynamic gate now requires one or more clocking inputs. This adds metallization and parasitic capacitance. An additional drawback to dynamic logic is that charge redistribution issues significantly impact the fan-out potential of a circuit. The output "floats" high since it is not being driven statically by the supply voltage, thus every gate that draws on the output pulls that output voltage lower. If the output feeds too many subsequent gates with excessive associated capacitance, the charge sharing will result in the output signal being pulled so low that its proper value is lost.

The effect of increasing the fan-out of a gate can be seen in the HSpice simulation of Figure 4 in which a TDFL inverter with a switching EFET width of 6.0 μm and a 9.2x9.2μm capacitive EFET is tested driving fan-outs of 1, 2, 4, 6, and 12. Note that at 1.0, 2.0, and 5.0 ns the highest output value represents a simulated fan-out of one and the lowest, a fan-out of twelve. Clearly, the higher fan-out situation will experience reduced noise margins.

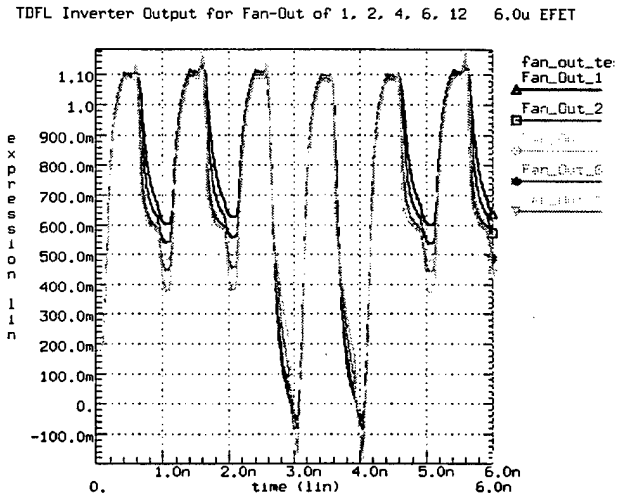


Figure 4 Simulation showing effect of Fan-Out on Output Voltage

3. Design Considerations

The design of GaAs dynamic circuitry demands that the engineer appreciate the clocking dependence and pipelining nature of dynamic logic and, perhaps more importantly, that they be aware of the charge sharing issues inherent in dynamic logic design. The designer can adjust FET sizes to accommodate several of these challenges. For example, if a larger fan-out is desired, the gate area of the reverse biased diode can be

increased, thus increasing its capacitance. This larger capacitance can then more adequately drive the input capacitances of the various gates being fed by the output but the penalty is that the RC time constant has increased and hence, circuit speed may suffer. It is not likely that the designer will want to use anything but minimum length FETs as to do otherwise would only increase the channel resistance unnecessarily. It may be useful to increase the width of the switching EFETs to achieve higher current and thus an output signal whose value can drop to a low state faster. The chief drawbacks of increasing the width of the switching EFET are increased layout area and increased gate and drain capacitance.

4. TDFL Topology

In Figure 3(b), one sees the non-overlapping clocks of this logic topology, hence the name "two-phase" dynamic FET logic. Looking at the TDFL inverter schematic of Figure 3(a), it was observed that when $\Phi 1$ is asserted the inverter is in the precharge stage. Retracting $\Phi 1$ and asserting $\Phi 2$ forces evaluation of the circuit. Q1, the pass transistor, serves to isolate the gate of the switching EFET, Q4, from the precharge phase of the output of the previous device, as well as trapping the charge at the gate of Q4 allowing proper evaluation during that phase. This gate voltage is stored on the small amount of gate capacitance of Q4 such that when $\Phi 2$ is asserted, Q4 can either pass or block the discharge of the output. Q5 acts as a reverse-biased diode to provide ample output capacitance thus boosting the fan-out of the gate. The higher capacitance was achieved by making the gate area of Q5 quite large, up to 84 μm^2 (9.2 μm x 9.2 μm).

Figure 5 shows the simple modification necessary to produce a TDFL 2-input NOR gate. As with GaAs DCFL, the NAND gate is generally avoided because of the negative impact of having the EFETs in series which increases overall channel resistance and thus reduces circuit speed and noise margins.

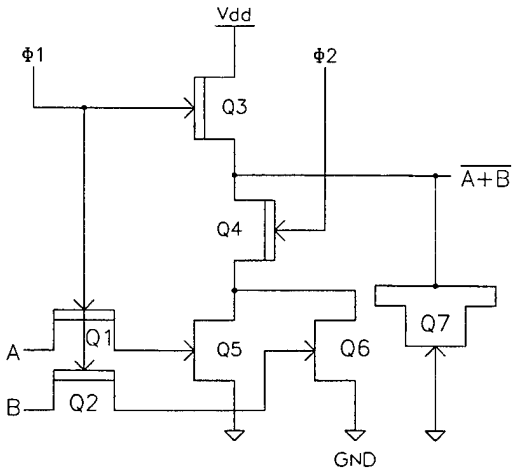


Figure 5 TDFL 2-input NOR Gate

The output of each TDFL gate is only valid during the evaluate phase. Therefore, it can be seen that the output of an inverter whose evaluate phase occurs when Φ2 is asserted will not be able to feed a TDFL gate whose precharge occurs during Φ1. Let a Φ1 gate be defined as one where precharge occurs when Φ1 is asserted and similarly for a Φ2 gate. It should be clear that to chain a series of TDFL gates, a Φ1 gate must precede a Φ2 gate which must precede a Φ1 gate and so on. This requirement for alternating the gates must be considered when designing and laying out the circuit.

This chapter has covered the main points necessary to understanding the execution of this thesis project. With a more basic understanding of GaAs as a semiconductor, the nature of GaAs MESFETs, and the DCFL and TDFL logic topologies, it is intended that the reader will possess a heightened appreciation for the design and testing of the chips documented in this thesis.

III. PSEUDO-NOISE SEQUENCE GENERATOR (PNSG)

A. BASIC DESCRIPTION

The function of the circuits designed in this thesis was that of a 7-bit pseudo-random number or pseudo-noise sequence generator (PNSG) which has applications in spread spectrum communications. These pseudo-random sequences are members of a class of codes termed maximal-length codes. These codes have the property that they represent the longest code or sequence which can be produced by a shift register of a given length. An n-bit shift register will produce a code of length 2^n-1. For example, with a shift register of seven bits, the code length is 2^7-1=127 bits long. The minus one accounts for the fact that one state is an illegal state which will not be entered barring an error in circuit operation. The sequence is termed "pseudo-random" because, to an unsynchronized receiver, the sequence produced appears to have a degree of randomness and unpredictability. If the number of bits in the sequence generator is large it can be very difficult to predict what the next bit will be, thus the sequence is "random" to the extent that predicting its behavior appears to be impossible. [6]

Because the sequence does repeat, an autocorrelation of the signal generated will produce strong returns at intervals that coincide with the length or period of the sequence. As the sequence length is increased, however, the power spectral density of the signal begins to approach that of white noise, hence the name pseudo-noise. This characteristic can be employed to great advantage in a number of communications systems for purposes of synchronization and encoding.

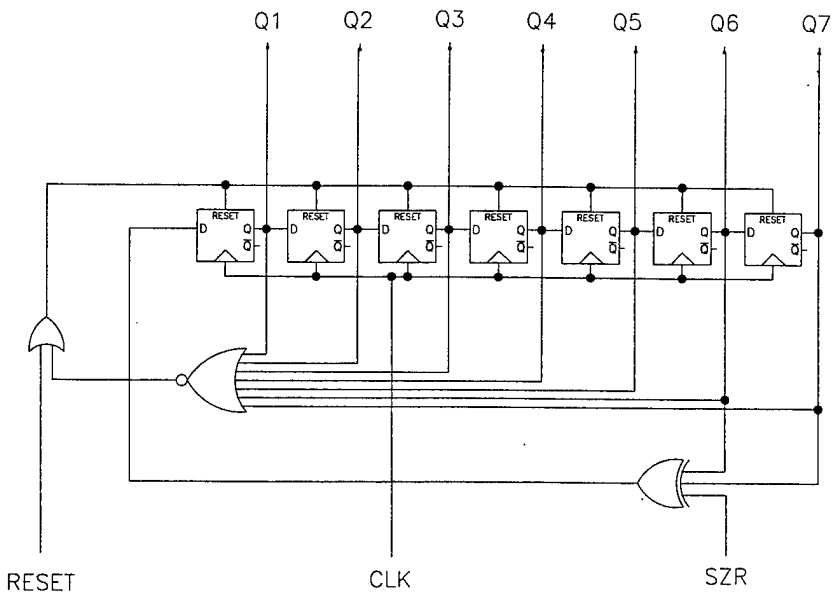


Figure 6 Basic PNSG Functionality

Figure 6 depicts a logic level schematic of the circuit designed for this research project. Note that the feedback is an exclusive-or or modulus-2 addition of the sixth and seventh bits. This structure is often referred to as a linear feedback shift register (LFSR). This is one way to produce a maximal-length sequence. There are other schemes which exist that produce different, but still maximal, length sequences. For example, if instead of feeding back the exclusive-or of the sixth and seventh bits, the seventh bit was XOR'ed with the first, third, or fourth bit and fed back, three new maximum length sequences would be produced. Using an exclusive-nor feedback will produce yet another set of sequences, the main difference being that the illegal state becomes all-ones vice all-zeros when using XOR feedback. In Table 1, the first several elements of the pseudo-random sequence can be seen and referencing Q6 and Q7 will reveal the next value of Q1.

Q1	Q2	Q3	Q4	Q5	Q6	Q7
0	0	0	0	0	0	1
1	0	0	0	0	0	0
0	1	0	0	0	0	0
0	0	1	0	0	0	0
0	0	0	1	0	0	0
0	0	0	0	1	0	0
0	0	0	0	0	1	0
1	0	0	0	0	0	1
1	1	0	0	0	0	0

Table 1 Sample of 7-Bit Pseudo-Random Sequence

B. ADDITIONAL FUNCTIONALITY OF PNSG

The schematic of Figure 6 produces the desired PN sequence and support some additional functionality. Specifically, the circuit was designed with the ability to be reset to a known state, to recover from an all-zero state, and to introduce an error on command.

The use of an asynchronously resettable flip-flop provided a solution to the requirement that the ability to set a known state exist. When the RESET signal is asserted, all seven flip-flop outputs are asynchronously set to a high logic value. This provides a mechanism for setting the LFSR to a known initial state which is a valid member of the pseudo-random sequence. This feature also proved useful in evaluating the performance of the chip during the testing phase of this thesis. The RESET signal was used both to reset the registers and simultaneously trigger the sampling oscilloscope.

A PN sequence should be capable of recognizing and correcting itself in the event that it enters the illegal state. For the LFSR of this thesis, an all-zero state is illegal. It can be seen that once in this state, the normal feedback mechanism will produce a

feedback of all zeros, thus perpetuating the state. The all-zero state can easily be identified and corrected using a seven-input NOR gate, the output of which can be used to assert RESET, thus setting the sequence to an all-high state.

For testing purposes, the circuit was designed with the ability to induce an error in the standard PN sequence. This error introducing signal, if properly timed, has the ability to set the all-zero state, or set zero, hence it is abbreviated SZR. In Figure 6 it can be seen that by XOR'ing the error introduction signal, SZR, with the standard feedback value of the LFSR, an error is introduced in the normal sequence. Because SZR can set the all-zero state, it provides a means by which the ability to recover from the all-zero state can be tested.

The PNSG is comprised of a basic linear feedback shift register (LFSR), a zero-detect and correct circuit, asynchronous reset to an all-ones state, and circuitry that permits the introduction of an erroneous bit into the sequence. That is the extent of the functionality of this chip. As will be discussed later, the only additions to this basic structure were meta-stability protection and superbuffers to insure sufficient internal current capacities.

IV. DCFL DESIGN, ANALYSIS, AND TESTING

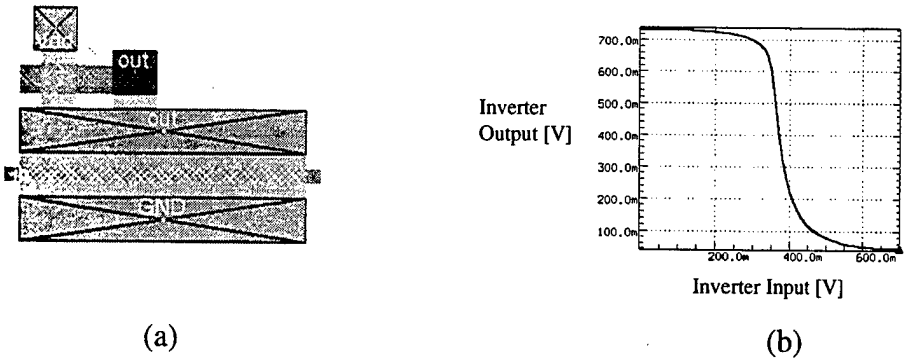
The first task of this thesis project involved the design and simulation of the DCFL version of the 7-bit PNSG. This stage required establishing familiarity with both the layout design software, Magic, and the HSpice circuit simulation tool. Upon completion of the layout and satisfactory simulation, the PNSG chip was submitted through MOSIS for fabrication by the Vitesse Semiconductor Corporation of Camarillo, California. After approximately five months, the completed chips were delivered and then tested for proper functionality, speed, and power consumption. This chapter details each stage of the design and testing of the DCFL PNSG.

A. LAYOUT

All of the layout design of this thesis was done using the Magic CAD software. The "hgaas3.tech" file was used by Magic to insure proper design rule checks, correct extraction to HSpice, and generation of a workable ".cif" file for fabrication, because the chips were to be fabricated using Vitesse Corporation's HGaAs III process. One feature of Magic that proved particularly helpful was the real-time design rule checking. Real-time DRC insured that the layout portion of the thesis progressed more quickly and that the layout produced complied with the Vitesse HGaAs III fabrication specifications.

One of the first goals in the layout process was to establish a library of basic gates which could then be pieced together to create other logic structures higher in the functional hierarchy. Fortunately, due to previous work in the field, the inverter and

2-input NOR gate already existed, though some minor modifications were made that improved the compactness of juxtaposed gates.



(a) (b)

Figure 7 DCFL Inverter (a) Magic layout (b) HSpice Transfer Curve

In Figure 7(a) the basic layout for the DCFL inverter is shown. Notice that the gate of the EFET is much wider and shorter in length (16μm x 0.8μm) than that of the DFET (2.0μm x 1.6μm). This was necessary to optimize the noise margins of the gate. Figure 7(b) shows an HSpice-generated transfer curve for the same inverter. Note the symmetry of the curve and the reasonably high gain of the drop off; these are responsible for generating optimal noise margins for the inverter. Using the unity gain point technique for calculating the noise margin of this inverter gives the values shown in Equations 1 and 2.

$$NM_H = |V_{OHmin} - V_{IHmin}| = |0.685 - 0.452| = 0.233 \text{ V} \quad \textbf{(1)}$$

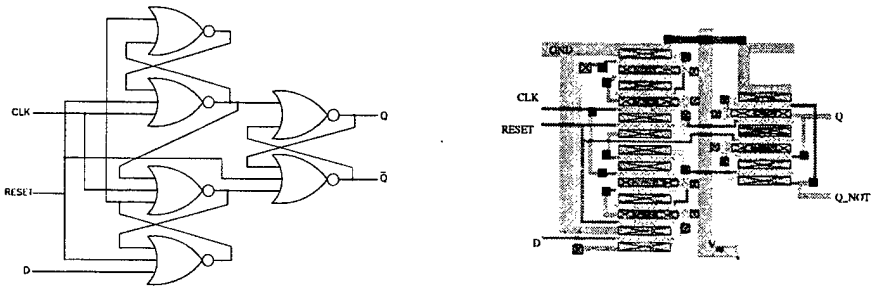
$$NM_L = |V_{ILmax} - V_{OLmax}| = |0.320 - 0.116| = 0.204 \text{ V} \quad \textbf{(2)}$$

It can be seen that DCFL GaAs has relatively low noise margins, in this case around 0.2V. These lower noise margins contribute to the challenge of GaAs design. All logic in the DCFL implementation was realized through the use of inverters and 2, 3, 4, and 7-input NOR gates.

B. HIGHER LEVEL STRUCTURES

1. Edge-triggered Resettable Flip-Flop

Since a PNSG is really just a series of flip-flops chained together with a simple feedback path, it was necessary to produce a DCFL flip-flop. As was previously mentioned, DCFL GaAs circuits operate best using NOR gates vice NAND gates because the gate employs switching EFETs in parallel rather than in series, thus increasing the speed with which the output drops from a high to low state. For this reason, the flip-flop was designed using only NOR gates. Further, it was desired that the flip-flop be asynchronously resettable. Therefore, functionality was added such that when RESET is asserted, the output, Q, is high. Figure 8 shows a schematic and layout of the derived circuit which delivers a falling-edge-triggered, asynchronously resettable, NOR-gate-driven, D flip-flop. This flip-flop utilizes four, 3-input, NOR gates and two, 2-input, NOR gates for a total of 22 FETs (16 EFETs and 6 DFETs). The fan-in of the D input is one unit of gate current. The CLK input has a fan-in of two, and the RESET input has a fan-in of three.



(a) (b)

Figure 8 (a) Schematic and (b) Layout of Edge-triggered FF implemented in NORs

2. 7-Bit Register

After the flip-flop was designed and simulated to confirm proper operation, creating the 7-bit register was simply a matter of chaining 7 flip-flops together. Having done that, the register was then simulated to establish that the flip-flops were driving each other properly.

3. 3-Input XOR Gate

The feedback required for the PNSG is a 3-input exclusive-or gate with Q6, Q7, and SZR as inputs. Once again, the NOR gate was the logic tool of choice. The Karnaugh map in Figure 9 shows the four maxterms which make up the 3-input XOR.

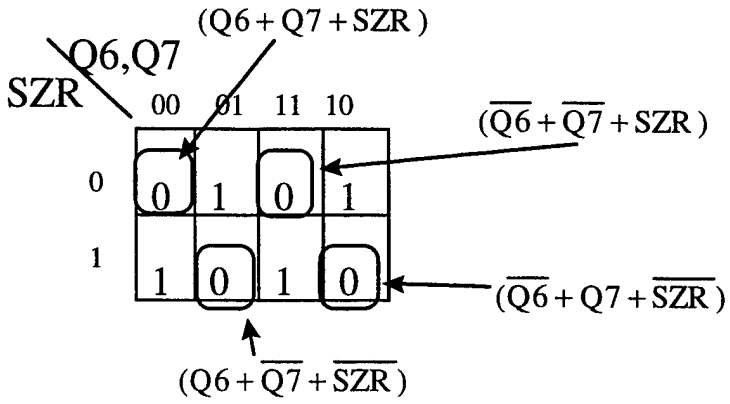


Figure 9 Karnaugh Map of 3-input XOR

$$Q6 \oplus Q7 \oplus SZR = (Q6+Q7+SZR)(Q6+\overline{Q7}+\overline{SZR})(\overline{Q6}+\overline{Q7}+SZR)(\overline{Q6}+Q7+\overline{SZR}) \quad \textbf{(3)}$$

From Equation 3, it can be seen using DeMorgan's Theorem that the function can be realized using only NOR gates as:

$$Q6 \oplus Q7 \oplus SZR = \overline{\overline{(Q6+Q7+SZR)} + \overline{(Q6+\overline{Q7}+\overline{SZR})} + \overline{(\overline{Q6}+\overline{Q7}+SZR)} + \overline{(\overline{Q6}+Q7+\overline{SZR})}} \quad \textbf{(4)}$$

The 3-input XOR is implemented in two layers of NOR gates which provide good speed performance, clearly better than placing two, 2-input, XOR gates in series. The schematic representation of this gate can be seen in the bottom right portion of the schematic of the LFSR in Figure 10.

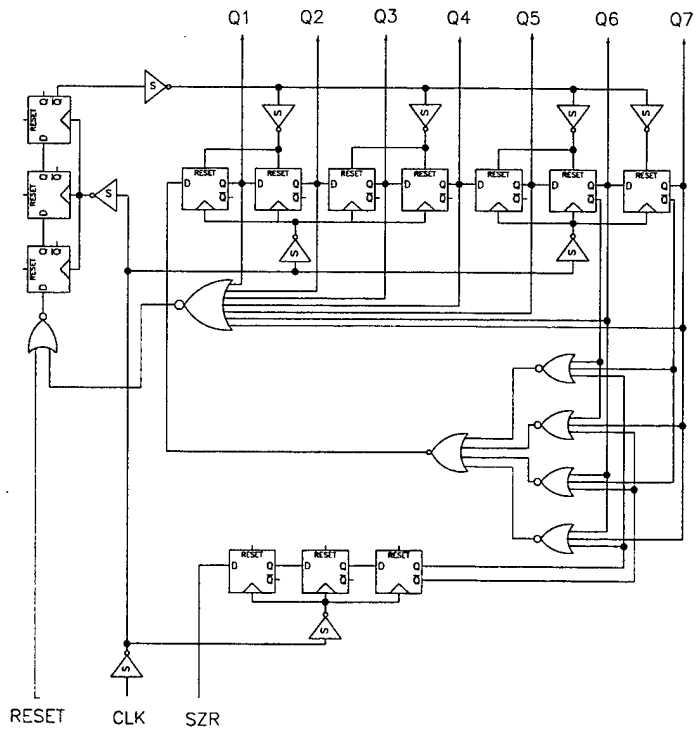


Figure 10 Schematic - DCFL LFSR

4. Meta-Stable Protection

The external input signals to the PNSG (other than the clock) are RESET and SZR. These signals may be asserted at any time and, consequently, there exists the possibility that the flip-flops driven by them could enter into an undesirable meta-stable state. To greatly diminish the risk that the seven flip-flops of the linear feedback shift register experience meta-stability, the RESET and SZR signals are first passed through a series of three D flip-flops. These buffering flip-flops effectively insure that the incoming signals are properly synchronized with the body of the linear feedback shift register. Although adding to the layout area, and more significantly to the delay between external

signal assertion and output response, it was felt that this protection was important to insure reliable operation of the PNSG.

5. Superbuffers

It was decided that superbuffers would be used for driving the 21 gate inputs of the RESET line and the 26 gate inputs for the clocking of the 13 flip-flops because these portions of the circuit draw higher current. The basic schematic of an SBFL inverter is shown in Figure 11. The 3 EFETs of the superbuffer are minimum length, 0.8 μm, and 16 μm in width. A logical high output is now driven through a wide EFET. Therefore, this gate has a much higher current drive capacity than a DCFL inverter and its use proved effective in the PNSG.

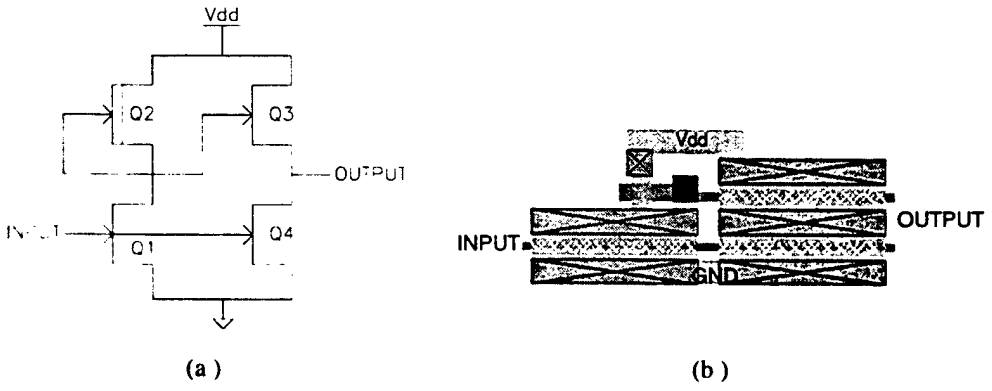


Figure 11 Superbuffer (a) Schematic (b) Magic layout

In Figure 12, we see the completed layout of the linear feedback shift register. Note the 3-input XOR implemented in two stages of NOR gates in the lower right, the

meta-stable protection for the RESET and SZR signals, the 7-input NOR gate for all-zero correction, and ten superbuffers scattered within the circuit.

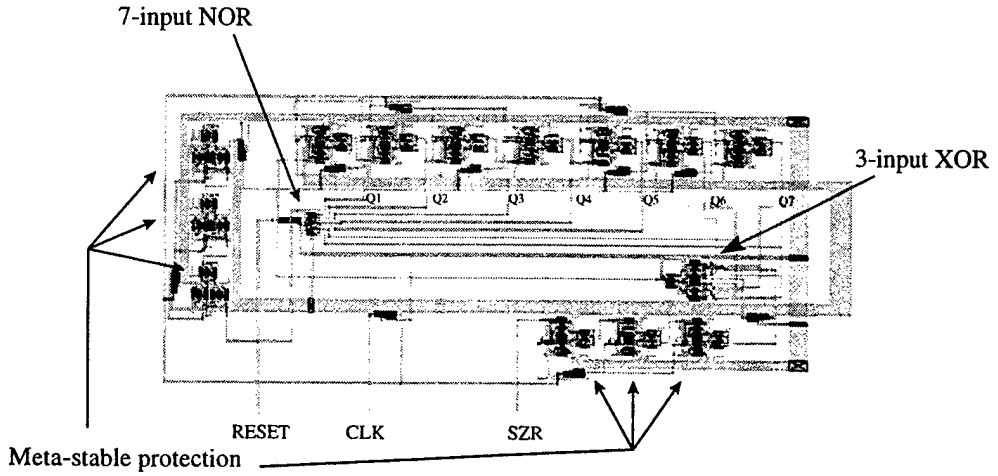


Figure 12 Layout - DCFL LFSR

6. Pad Ring

After the entire LFSR was completed with its error-correcting circuitry, meta-stable protection, and superbuffer drivers, it was placed inside a pad ring which enables the connection between the external chip package and the internal circuitry. The external signals RESET, CLK, and SZR are delivered to the inner circuit through pad ring receivers and Q1-Q7 are transmitted outside the chip through pad ring drivers. The receivers serve to protect the inner circuit from external hazards and the drivers insure sufficient current capacity to external circuits. This ensemble of LFSR and pad ring was then referred to as the PNSG. The layout of the entire chip, including the pad ring, can be seen in Figure 13. This layout, measured from the outer edges of the bonding pads was 1.25 x 2.3 mm. The internal circuitry measured 454 x 1085 μm. As can be seen, little

effort was made to compact this circuit because its relative simplicity meant that the pin-out would drive the size of the layout.

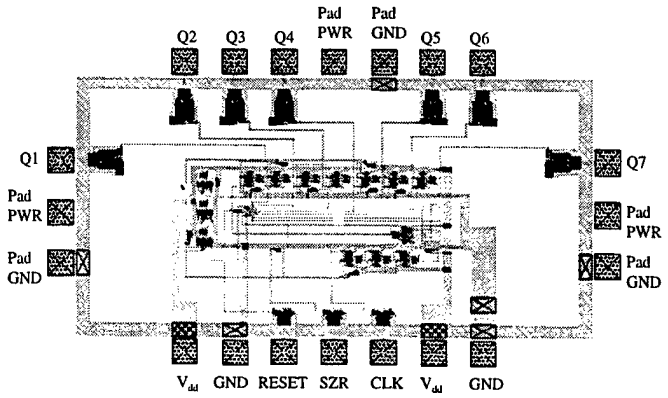


Figure 13 - Completed DCFL PNSG layout

The final step related to the layout of the chip was creating a bonding diagram so that MOSIS knew how to connect the fabricated chip to the 28-pin LDCC28 package. A copy of this bonding diagram is shown in Appendix A.

C. SIMULATION

The Magic CAD system is capable of extracting a layout and then generating an HSpice file from that extracted file. This was the method by which the HSpice simulation files were created, as opposed to creating HSpice logic gate units and building up the model from those units. This insured that the circuit being simulated was identical in function to the circuit laid out in Magic.

1. Extraction from Magic to HSpice

The extraction process produced HSpice files which required some modification to be compliant with the Vitesse HGaAs III process. Due to some inaccuracies in the extraction process, it was necessary to change some of the model numbers of the extracted FETs in the HSpice file. This work required that the following manual changes be made to the extracted HSpice files. First, extracted EFETs of length greater than 1.1 μm were changed from the "enh.1" model to the "enh.2" model. Second, extracted DFETs of length less than 1.25 μm were changed from the "dp1.2" model to the "dp1.1" model. And third, extracted DFETs of length 2.0 μm or more were changed from "dp1.2" to "dp1.3." These corrections were easily accomplished using a simple "search and replace" on the file. The only other steps required for simulation were to provide the HSpice code to specify Vitesse HGaAs III FETs, define the power supply voltages and input signals, and stipulate the type of simulation analysis desired. In the case of the DCFL circuits, V_{dd} was generally set to 2.0V but was adjusted as necessary to investigate circuit characteristics. Pad power took values from 1.0 to 2.0V and the external inputs swung between 0 and 1.2 volts.

2. Incremental Simulation Process

Once the HSpice file was groomed for execution the simulation was performed. The process of designing the circuit involved creating each component gate or series of gates and then simulating its performance. If the simulation showed deficiencies in the component performance, appropriate modifications were made until the design performed

as desired, at which point it could be used in the next higher component in the hierarchy. The initial simulations of the basic gates ran fairly quickly, sometimes in seconds, but the completed PNSG layout required several hours to analyze for a period of 50 ns at a temporal resolution of 10 ps.

3. Simulation Results

The LFSR (the circuit prior to insertion into the pad ring) simulated successfully at 2 GHz. A portion of the PN sequence can be seen in the simulation in Figure 14 below.

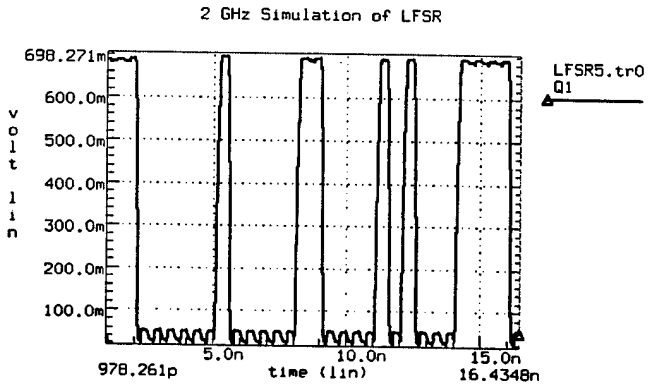


Figure 14 Simulation of LFSR at 2 GHz

Though critical to creating a packaged implementation of the PNSG, the output drivers of Q1 through Q7 were the limiting factor in the maximum speed of the circuit. With the pad ring and its associated output drivers and receivers, the maximum simulated speed fell to 1.2 GHz.

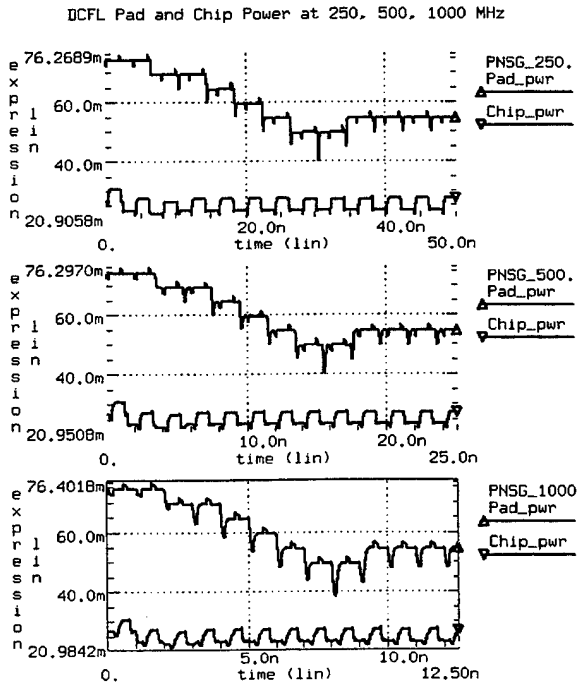


Figure 15 DCFL HSpice Simulation showing power independent of frequency

One characteristic of the DCFL chip that was revealed by simulations and later confirmed by actual testing was that internal chip power consumption was virtually independent of clock frequency, given that the pad power supply and chip power supply were held constant. This is revealed in Figure 15, showing the internal chip power at 250, 500, and 1000 MHz with chip power set at 1.5 volts and pad power at 1.0 volts. The upper trace in each plot is the power consumed by the pad ring and its associated receivers and drivers and the lower, more stable trace is the power consumed by the circuitry inside the pad ring. The pad ring consumes more than twice the power of the internal chip which averages 25 mW. The instantaneous power consumption of the pad ring depends largely on how many of the output drivers are transmitting a logic high because they drive a large current through the 50 Ω terminating resistors. The frequency

independence of the power consumption is a result of DCFL's high static power consumption relative to its dynamic power consumption. That is to say, the power consumption resulting from the static flow of current through the FETs is much greater than the dynamic current associated with the charging and discharging of the FET capacitances.

D. TESTING

The design and simulation analysis of the DCFL version of the PNSG was completed in early October 1996 and the associated .CIF file was subsequently submitted for fabrication to the Vitesse Semiconductor Corporation. Twenty fabricated chips were received in March 1997. The next logical step was to test and evaluate the fabricated chips. The twenty chips delivered included 10 chips created using the standard Vitesse HGaAs III process and 10 more fabricated using an experimental wafer with a low temperature GaAs (LT GaAs) buffer layer. Vitesse reported that the fabricated EFETs of minimum length, 0.8 μm, were measured to have a threshold voltage, V_T, of 0.28V and V_T for the DFETs was measured to be -0.84V.

1. Test Board

The first step in the testing process was to design and build a test board for the completed chips. The test board that was used was a computer board with a thin layer of copper already laid out in the proper pattern. Onto this board were soldered the various connectors which formed the inputs, outputs, and power and ground lines of the PNSG.

The three input lines, RESET, CLK, and SZR were connected with 50 Ω resistors between them and ground for purposes of impedance matching with the output drivers of the signal generators. All power lines, both pad power and chip power, were noise filtered with 0.01 μF capacitors to ground. The signals were routed on RG 174 coaxial cable with SMA connectors. These were chosen because of their excellent high frequency performance.

2. Test Equipment Configuration

Once the test board had been built, it was then necessary to connect the circuit to the appropriate power supply sources, signal generators, and sampling oscilloscope. A particularly challenging aspect of the testing involved trying to determine how best to trigger the circuit such that the pseudo-random sequence could be observed. Several possibilities were considered and/or tried. The first idea involved attempting to use the trigger output of the signal generator to apply the RESET signal to the circuit. This failed because the trigger output was of insufficient strength to drive the RESET signal. The next idea attempted was to boost the trigger output and add a DC offset in the continued hope that the trigger signal could drive the RESET. While this did provide some improvement, the result was still an unacceptable triggering condition.

The method which proved to be effective was to use a separate signal generator, the HP 8082A, to create both the o-scope trigger input and the RESET signal. Finally, using this method, a clear trace of the pseudo-random sequence was obtained.

The next challenge was determining how to test the all-zero correcting feature of the chip. From simulation experience, it was known that a properly timed SZR input could induce an all-zero state in the circuit. To employ this technique required the use of another signal generator, in this case an IEC (Interstate Electronics Corporation) Series 20 Pulse Generator model P25. This signal generator was able to produce a pulse with a minimum pulse width of 10 ns which was sufficient to produce the all-zero state in the PNSG. Using the DELAY adjust knob of the signal generator allowed the SZR signal to be asserted at just the right point in the sequence to produce an all-zero state. This effect was tested successfully up to a speed of 600 MHz.

The final test equipment configuration is depicted below in Figure 16. Having produced a workable configuration, the next step was to evaluate the performance of the fabricated chips.

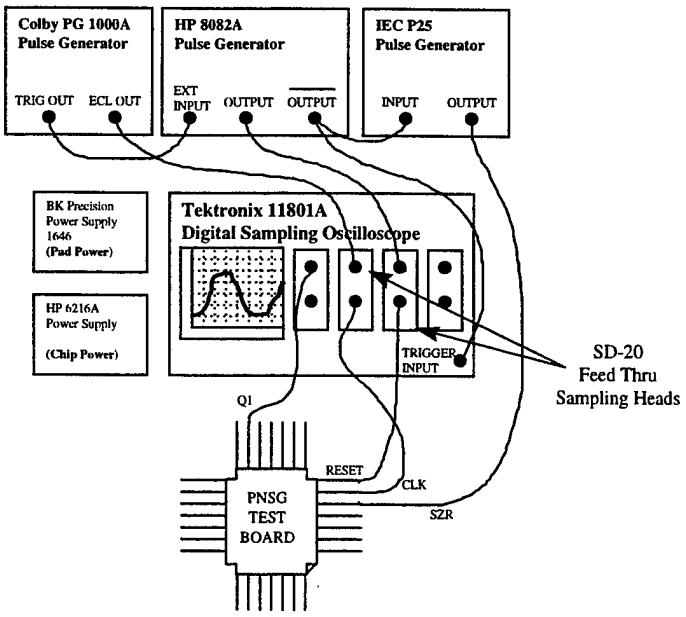


Figure 16 DCFL PNSG Test Setup

3. Test Results

The testing of the chips initially involved confirming that they operated properly, and then investigating the maximum speed and power consumption of each chip. All ten of the chips fabricated using the Vitesse standard HGaAs III process were functional, though their maximum speeds varied between 700 and 950 MHz. None of the ten chips fabricated using the LT GaAs wafers were found to function at all. Figure 17 shows that it was possible to produce the proper pseudo-random sequence at clock speeds nearing 1 GHz but to obtain these fast clock speeds required that the pad power level be reduced dramatically below the nominal 2.0 volts used in design and simulation. When running above 900 MHz the pad power supply was typically set to a value of approximately 0.6V and the internal power supply, V_{dd}, was set to 1.5V.

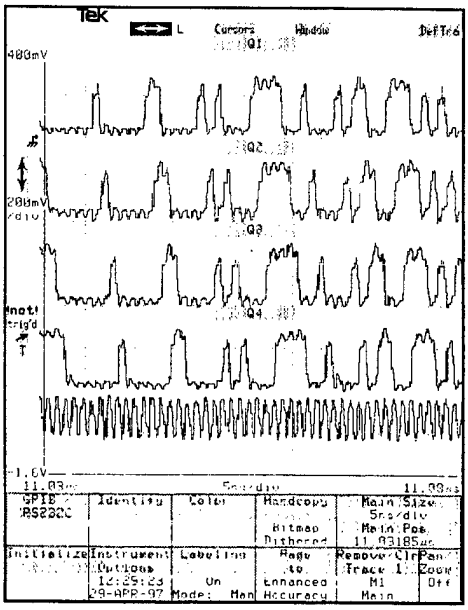


Figure 17 Q1-Q4 at 958 MHz

At these higher clock rates, the circuit was very sensitive to changes in supply power. Minor adjustments precipitated unusual changes in circuit performance. At any frequency, the rise and fall times of the output waveforms were observed to be 200 ps or less. This can be seen in Figure 18 showing the o-scope capture of chip #7 at 700 MHz with 500 ps per division.

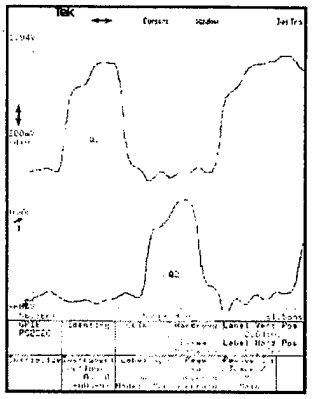


Figure 18 Output waveform showing 200 ps FT

In Figure 19, the all-zero correcting feature of the chip is demonstrated at a frequency of 600 MHz. This oscilloscope capture shows, from top to bottom, Q1, Q4, and Q7. Note that immediately to the left of the center of the trace, all three signals are at logic lows, as are Q2, Q3, Q5, and Q6. Closer inspection of the Q7 signal reveals that the outputs are all low for three clocks cycles while the internally generated reset signal propagates through the three meta-stable protecting flip-flops. Immediately to the right of the center, the internally generated reset signal has now propagated through the meta-stable protection and is being simultaneously asserted to drive all output signals high. It then takes three more clock cycles for the reset signal to complete its propagation through the meta-stable protection circuit, thus allowing the LFSR to return to its normal PN sequence.

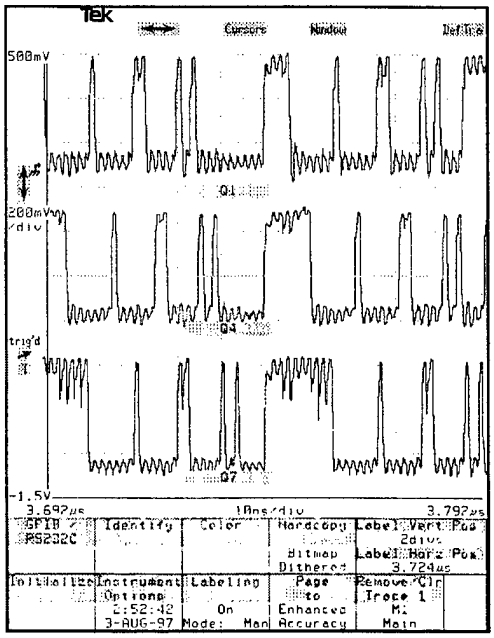


Figure 19 All-Zero Correction at 600 MHz

Figure 20 shows a comparison of a simulated and actual oscilloscope output for the circuit at 705 MHz. Note that in the o-scope view there is an increased delay between withdrawing the RESET assertion and Q1 going low (12 ns vs 6 ns). This effect is primarily due to 40 cm of RG 174 coax between the oscilloscope feed through sampling head for the RESET signal and the test chip added to 60 cm more between the chip and the Q1 sampling head. This 100 cm of cabling introduces 5 ns of additional delay. As expected, the simulated waveform is cleaner in appearance than the actual signal.

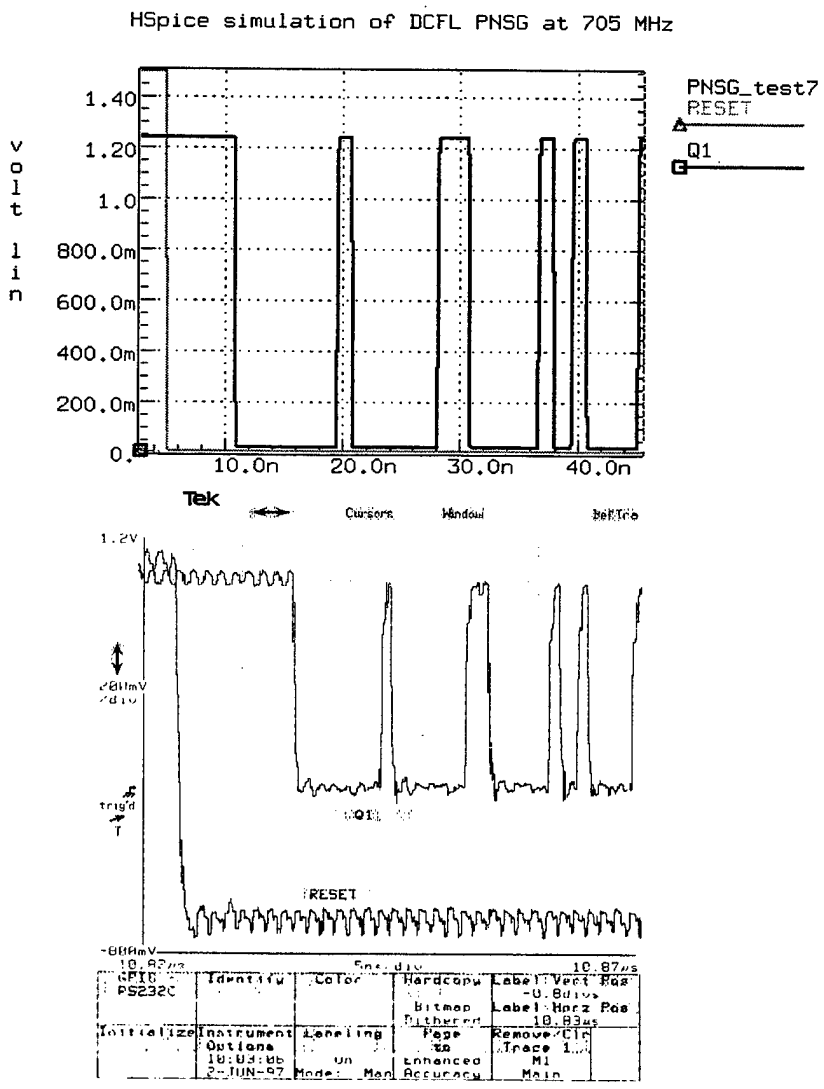


Figure 20 Comparison of HSpice Simulation and Circuit Run at 705 MHz

Table 2 shows the test results of the ten standard process (non-LT) chips. The chips were numbered arbitrarily and then tested for proper functioning and speed. All ten chips operated properly, though as can be seen, some ran considerably faster than others. As previously stated, all but one chip required low power levels to obtain high (>700 MHz) clock rates. Chip #2 was unusual in that it not only accepted, but required a very

high value for V_{dd} in order to run at high speeds. Note that at 760 MHz, V_{dd} was set to 5.76 V but its chip current was not correspondingly elevated.

Chip #	Max Clock [MHz]	Chip V_{dd} [V]	Chip Curr [mA]	Pad Volt [V]	Pad Curr [mA]	Output Amplitude [V]
1	701	1.19	20.3	0.86	44.9	0.4
2	760	**5.76**	29.7	1.72	74.7	**0.8**
3	800	0.99	18.6	0.89	37.6	0.5
4	757	1.09	20.3	1.52	81.3	0.65
5	925	1.54	25.55	0.63	35.7	0.3
6	702	0.86	15.8	0.87	42.7	0.4
7	709	1.18	19.4	1.51	75.6	0.83
8	**976**	1.48	26.0	0.58	37.1	0.25
9	916	1.54	26.9	0.89	66.3	0.4
10	801	1.54	23.7	1.11	56.2	0.55

Table 2 Maximum Speed Data for non-LT DCFL PNSGs

In agreement with the HSpice simulations, the power of the chip was virtually independent of clocking frequency. This can be seen in Figure 21, which shows the internal chip power consumed as a function of frequency and chip supply voltage, V_{dd}. This data set was obtained on chip #8 by holding the pad power supply steady at 1.0 V and then increasing V_{dd} from 0.75V to 2.25V in 0.25V increments. With each value of V_{dd}, the clock frequency was stepped through 50, 100, 200, 300, 400, 500, 600, 700 MHz and up to the maximum frequency of operation for the set power supplies.

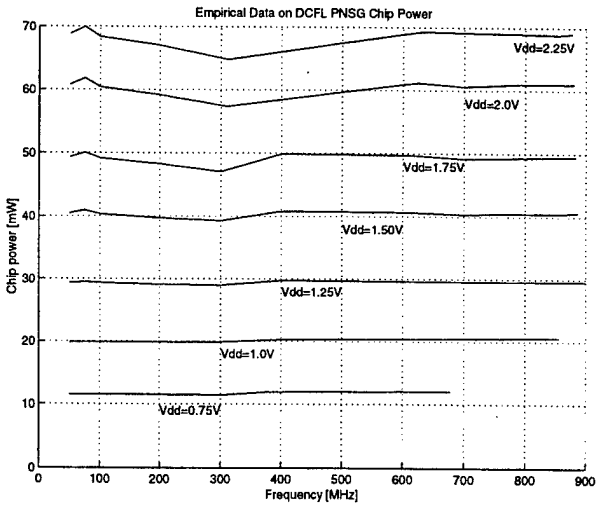


Figure 21 Chip #8 Power Consumption

As stated above, the LT GaAs chips failed to show any sign of functionality. The testing of these chips involved the same test setup which had proved effective in running the non-LT chips. At a clock speed of 10 MHz, the chips were tested by successively setting the chip power supply to 1.0, 2.0, and 3.0 volts and then sweeping the pad power supply from 0.5 to 3.0 volts. The outputs Q1-Q7 were monitored and found to remain at a high logic value. There was no sign of any of the signals changing value. It was interesting to note that the current drawn by the internal chip was approximately five times less than that of the non-LT chips for the same supply voltage. This effect may have been due to a significantly higher threshold voltage in the LT chips.

Overall, the positive performance of the DCFL chips was very encouraging, particularly their strong performance at frequencies nearing 1 GHz. Because the TDFL chip has not yet completed fabrication, comparisons between the DCFL and TDFL will be based on simulation results of the TDFL design.

V. TDFL DESIGN AND ANALYSIS

Having completed the design of the DCFL version of the chip and submitted it for fabrication, the next objective was to begin the design of the TDFL chip. The layout and simulation of the TDFL design were similar to the DCFL design because the same software tools were used, Magic and HSpice. The TDFL design introduced the additional challenges of heightened fan-out awareness, designing pipelined logic, and orchestrating a two-phase clocking strategy. Fortunately, the shift register at the heart of the PNSG lends itself to this type of design. Overall, the process was basically the same, involving laying out and simulating progressively more complex components until the entire TDFL circuit was completed.

A. LAYOUT

Magic continued to be the layout tool as the TDFL circuit was designed. Unlike the DCFL chip, however; there was no library of dynamic gates from which to borrow so one was created. Fortunately, the number of basic gates that were to be designed was minimal, consisting of an inverter, 2 and 3-input NOR gates, and a 2-input XNOR gate.

1. TDFL Inverter

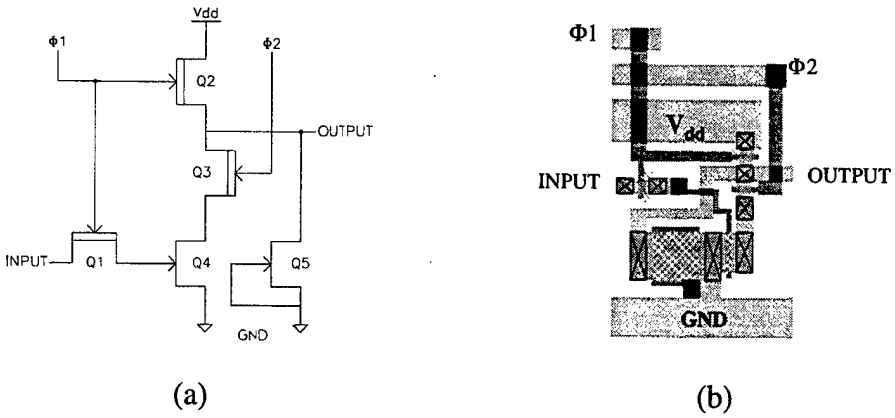


Figure 22 TDFL Inverter (a) Schematic (b) Layout

Figure 22 shows the schematic and layout for the TDFL inverter. Notice that the DFETs are all minimum size (0.8 μm long by 2.0 μm wide) because this provides minimum input capacitance and layout area, and because precharge speed was not a limiting factor. The EFET, Q4, is minimum length but is somewhat wider than minimum at 6 μm to provide a more rapid discharge path to ground during evaluation. Figure 23 is an HSpice simulation showing the effect of varying the width of Q4 on a dynamic inverter driven at 1 GHz. There are three curves in the plot, the highest and darkest being a sample of the output when the EFET is 2 μm wide, the next curve is with a 3.2 μm width, and the lowest and faintest with a width of 6 μm. Note that as the width is increased, the signal drops off to a logic low faster which is a positive effect. The primary disadvantage in using a wider EFET is that the logic high value is reduced due to the increased drain capacitance of the EFET and the increased gate capacitance of the switching EFET of the following TDFL gate. This adversely impacts noise margins and the greater width increases layout area. HSpice simulations revealed that output

discharge to a logic-low was the limiting factor in the speed of the TDFL circuit. For this reason, it was decided that the 6 μm width would be used because it provided excellent evaluation speed for logic-low outputs while offering acceptably high logic-high output.

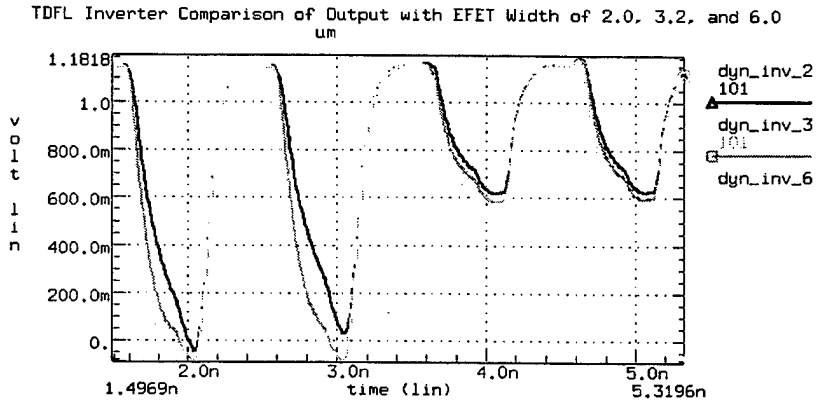


Figure 23 Simulation showing effect of varying width of switching EFET, Q4

The purpose of Q5 in the TDFL inverter of Figure 22(a) is to provide output capacitance for driving successive gates. This large gate-area (7.2 μm x 7.2 μm) EFET can be seen in the bottom left portion of the layout in Figure 22(b). While the configuration shown in Figure 22(a) does provide ample capacitance, HSpice simulations show that greater capacitance would have been realized by using the reverse-bias diode configuration depicted in Figure 3(a) on page 15. HSpice simulations show that for square gate areas, the reverse-bias diode configuration carries 14% greater capacitance than that shown in Figure 22(a). The gate area of Q5 was varied depending on the required fan-out of the gate. The largest fan-out of any dynamic gate in the circuit was four gate inputs. It was found that an 84 μm^2 gate area for Q5 was sufficient to drive this fan-out while maintaining a minimum output logic-high voltage of 0.5V. This provided good TDFL noise margins.

2. TDFL 2 and 3-Input NOR Gates

Figure 24 shows the schematic diagram and layout for a 2-input, TDFL, NOR gate. In this gate, like the inverter, the switching EFETs, Q5 and Q6, were made 6 μm wide to allow rapid evaluation to a logic-low output. The output, capacitance-boosting EFET, Q7, was made 7.2x7.2 μm or 9.2x9.2 μm depending on the load being driven by the output. The 3-input NOR gate is a simple extension of the 2-input NOR.

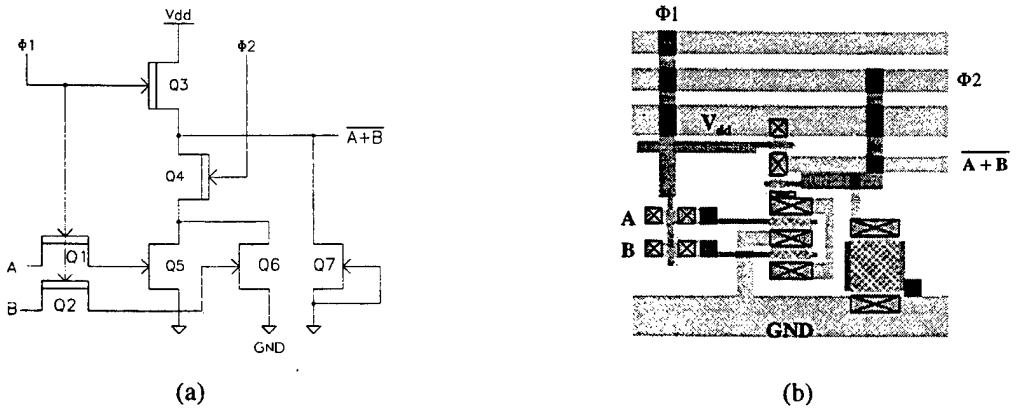


Figure 24 TDFL 2-Input NOR (a) Schematic and (b) Layout

Figure 25 shows an HSpice simulation of the 2-input NOR running at 1 GHz. In this particular TDFL gate, Φ1 is the precharge phase and Φ2 signals evaluation. Note that the proper output voltage of the NOR gate is obtained while Φ2 is asserted and that the output-high voltage never drops below 0.5V.

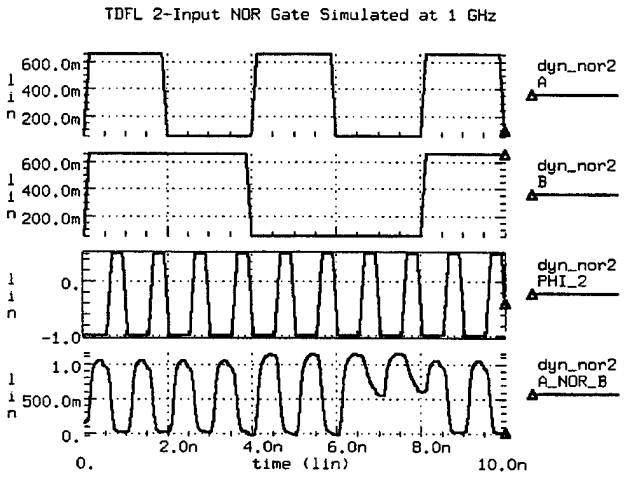
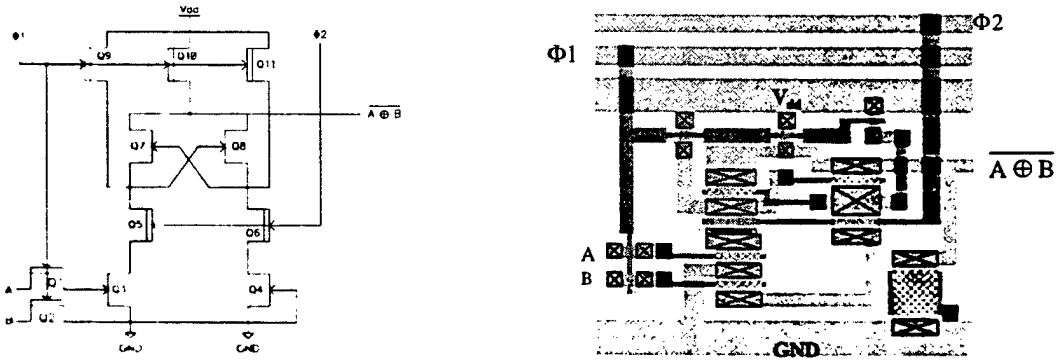


Figure 25 Simulation of TDFL 2-input NOR at 1 GHz.

3. 2-Input XNOR Gate



(a) (b)

Figure 26 TDFL XNOR (a) Schematic and (b) Layout

The PNSG utilizes a 3-way exclusive-or as its feedback, therefore, it was necessary to produce this functionality in TDFL logic. From Reference 2, a schematic was detailed for a TDFL XNOR gate. Figure 26 shows the schematic diagram and layout

for this gate. This gate requires that the output discharges through two EFETs and a DFET to reach a logic low during the evaluation phase. To accommodate a rapid discharge, the gate widths were increased making Q5, Q6, Q7 and Q8 8.0 μm wide and Q3 and Q4 were 7.2 μm wide. By following this gate with a TDFL inverter, a TDFL XOR gate is realized. A simulation of such an XOR gate clocked at 1 GHz is shown in Figure 27. Notice the lag in the output due to the phase delay of the complimentary TDFL gates. Pipelining two XOR gates in series achieves the effect of a 3-input XOR gate as desired.

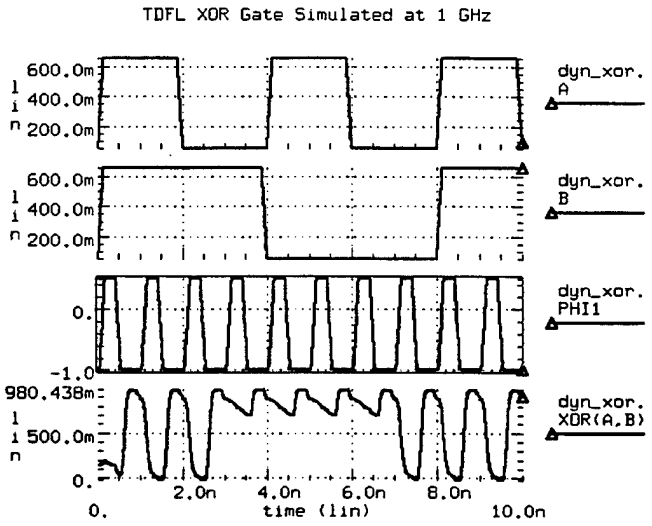


Figure 27 Simulation of TDFL XOR at 1 GHz

B. HIGHER LEVEL STRUCTURES

1. Dynamic Resettable Flip-Flop

In order to obtain the effect of a sequence of registers, it was necessary to create a register-like structure. Dynamic logic is, by its very nature, clocked. Therefore, to create

a dynamic flip-flop simply required putting two dynamic inverters in series with the output of the second inverter being essentially the same as the Q output of a standard D flip-flop. The only enhancement that was necessary was to enable this dynamic flip-flop to be reset asynchronously.

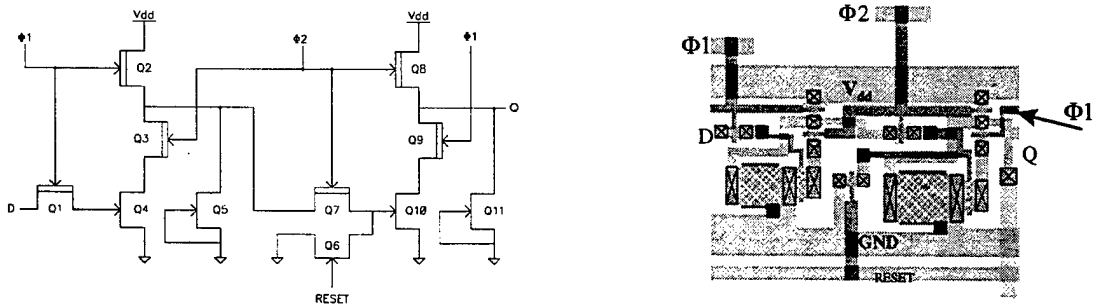


Figure 28 TDFL Flip-Flop (a) Schematic (b) Layout

In Figure 28(a), transistor Q6 was added to provide this reset capability. It can be seen that if the RESET signal is asserted high, the transistor, Q6, is turned on, which forces Q10 off, thus the output Q will float high during the evaluation phase. Note, in the layout of Figure 28(b), that the gate area of Q11 (9.2μm x 9.2μm) is larger that that of Q5 (7.2μm x 7.2μm). This is the case because the final output drives a larger capacitive load than the first TDFL inverter, which only drives the second inverter.

2. Two-Phase Clock Driver

In order to create a more functionally complete TDFL PNSG chip, it was decided to implement a two-phase clock driver on-chip to produce the non-overlapping internal clock signals. Figure 29 shows the schematic, layout, and simulated output of the circuit

used to produce the clock driver and the associated layout. To insure the non-overlapping characteristic, the cross-feedback into the NOR gates was fed through two inverters which created the necessary delay. To produce the negative offset in the two-phase clock outputs, the signals were pulled down using a source-follower series of DFETs to a V_{ss} supply voltage of -2V. Figure 29(c) shows that the simulated output voltage swings the desired -1.0 to 0.25V with no overlap. Close inspection of the output waveform reveals that the $\Phi 2$ pulse is narrower than the $\Phi 1$ pulse. This occurs because of the front-end inverter in the clock-generator circuit which has some finite propagation delay. At 1 GHz this effect is negligible, but at frequencies above 1.2 GHz the effect becomes problematic, resulting in the decay of $\Phi 2$ while $\Phi 1$ is still of sufficient amplitude.

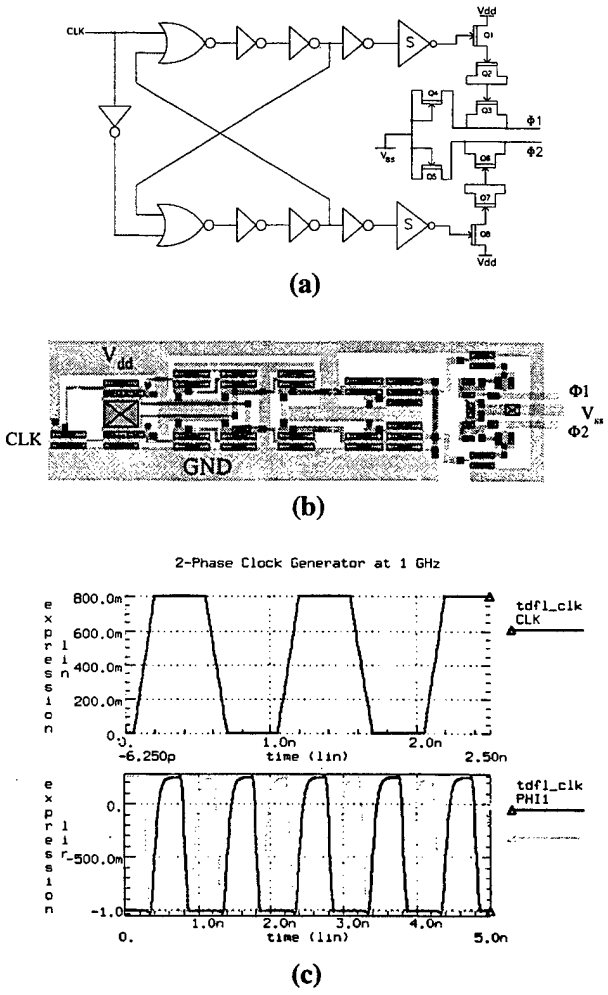


Figure 29 Two-Phase Clock Generator (a) Schematic (b) Layout (c) Simulation

3. Linear Feedback Shift Register

Creating the LFSR required that the dynamic flip-flops be aligned in series and then fed back appropriately. The TDFL XOR gates described previously were used for the standard feedback. To produce the all-zero correcting circuitry required a combination of 2 and 3-input NOR gates. A 7-input, TDFL, NOR gate was not undertaken because the capacitive load of the drains of the seven switching EFETs would

have dragged the output down excessively. Figure 30 shows a schematic of the TDFL LFSR.

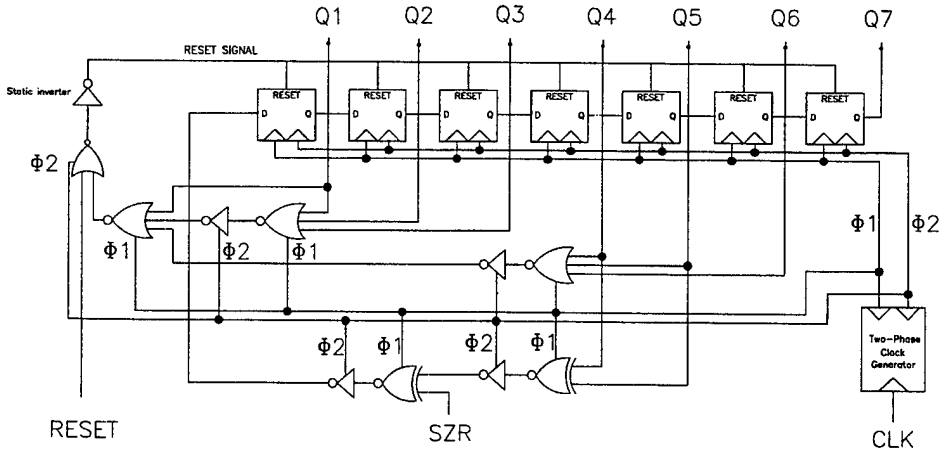


Figure 30 TDFL PNSG Schematic

Note that the output of the final dynamic flip-flop, Q7, is not used. This is a result of the pipelined nature of dynamic logic. Because every dynamic gate is clocked, the feedback delay is increased such that two cycles elapse (one cycle per XOR gate) before the feedback arrives at the input of the first flip-flop. To account for this delay, the feedback originates from Q4 and Q5 rather than Q6 and Q7, as was the case in the DCFL chip. The all-zero correction logic was implemented in the form of two, parallel, 3-input OR gates (TDFL NOR followed by TDFL inverter) which took Q1 through Q6 as inputs, then these two outputs and the updated value of Q1 were fed into a 3-input NOR. This arrangement produced the logical equivalent of NORing Q1-Q7. The static inverter is used to capture and set the correct sense to the RESET signal, whether of internal or external origin, and hold its value for at least one clock cycle. This circuit worked well as is shown in the simulation captures of the next section.

The final flip-flops, Q6 and Q7, were not needed to produce the PN sequence. Q6 was used in the logic for all-zero correction, but with the minor circuit modification shown in Figure 31, its use could have been eliminated. This improved circuit was not implemented, though it is more economical than the circuit delivered for fabrication and it restores the proper sequence one cycle faster after an all-zero state is experienced. In this circuit, the output of the feedback logic is used in the all-zero correcting logic, thus eliminating the need for Q6. This illustrates how the pipelined nature of dynamic logic may be exploited in certain applications to reduce the number of storage elements.

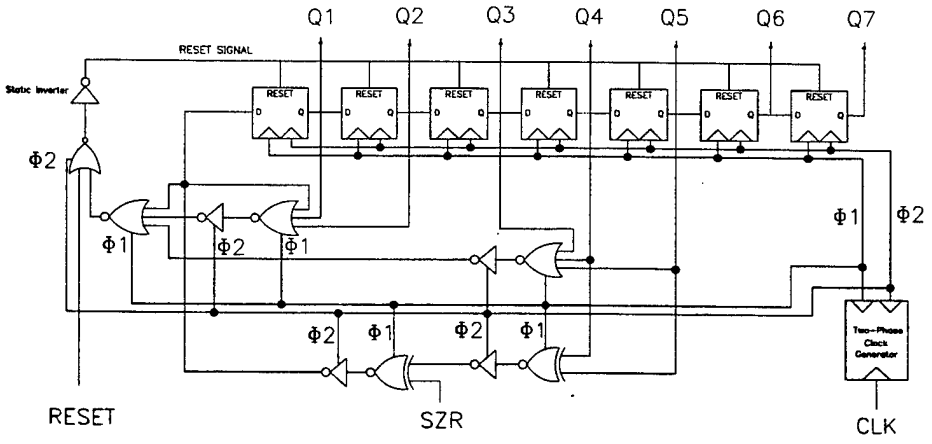


Figure 31 Improved TDFL Schematic (Q6 and Q7 not required)

The final layout of this circuit with its internal LFSR and outer pad ring with receivers and drivers is shown in Figure 32. This circuit was compacted to a greater extent than the DCFL chip but like the DCFL design, minimizing layout area was not a priority. The inner portion of the chip which excludes the pad ring and bonding pads measured 290 x 575 μm. The entire chip measured from the outside of the bonding pads

measured 833 x 1670 μm. It was this entire layout that was extracted to an HSpice file for simulation.

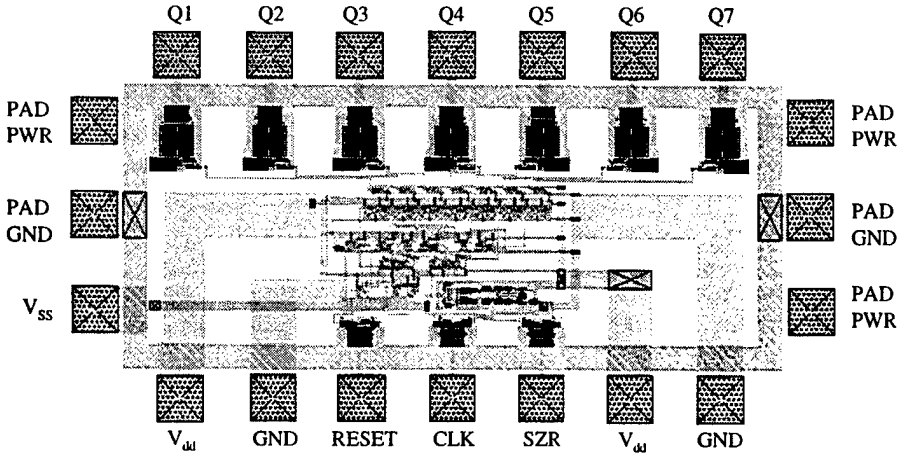


Figure 32 Layout of TDFL PNSG

C. SIMULATION

After the extracted HSpice file was adjusted to account for the minor inaccuracies of the Magic extraction process described in Chapter IV, the circuit ran through numerous HSpice simulations. These simulations first confirmed that the circuit exhibited the proper functionality, then speed and power consumption were examined more closely. Figure 33 shows a simulation of the TDFL PNSG at 1 GHz. This simulation shows the functionality of the error-introducing capability provided by the SZR input, the all-zero correction capability, and the standard PN sequence. Notice the pseudo-random pattern seen in output Q1 after 11ns. Though not shown in the plot to reduce clutter, the SZR signal was asserted from 6.1 to 7.4 ns in the simulation, thus inducing an all-zero state at

10 ns. Within one cycle of the all-zero state existing, the reset signal is asserted and all output signals are reset high at 11 ns and the normal PN sequence is reestablished. Internally, the TDFL signals had logic-high values of at least 0.5V and logic-low values of 0V or less which provided good TDFL noise margins. The internal TDFL signal for Q4, which had the highest fan-out demand of any flip-flop, can be seen in the center plot of Figure 33. Notice that its lowest high is above 0.5V.

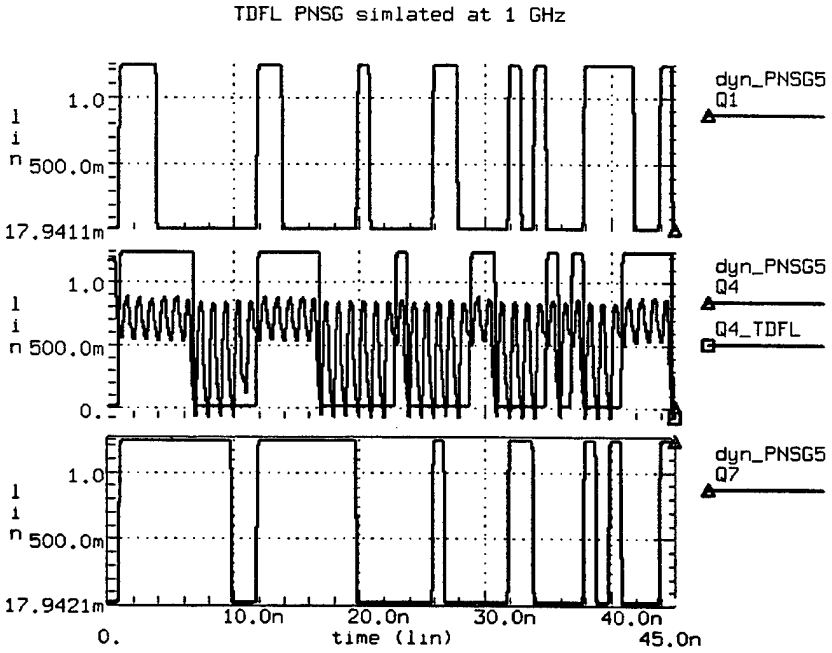


Figure 33 Simulation of TDFL PNSG at 1 GHz

The power consumption of the TDFL design was determined through HSpice simulation as well. In Figure 34, the internal chip power is plotted as a function of frequency. This particular data was obtained through a series of simulations with V_{dd} set at 1.5V and pad power at 1.0V because these values proved effective when running the

DCFL chip. Unlike the DCFL chip, there is a more significant increase in power with increasing frequency. Because the TDFL chip consumes substantially less static power, the dynamic power comprises a much larger percentage of total power. In general, the HSpice simulations show that the internal TDFL chip consumes an average of 8.2 mW compared with 25 mW for the functionally equivalent DCFL PNSG.

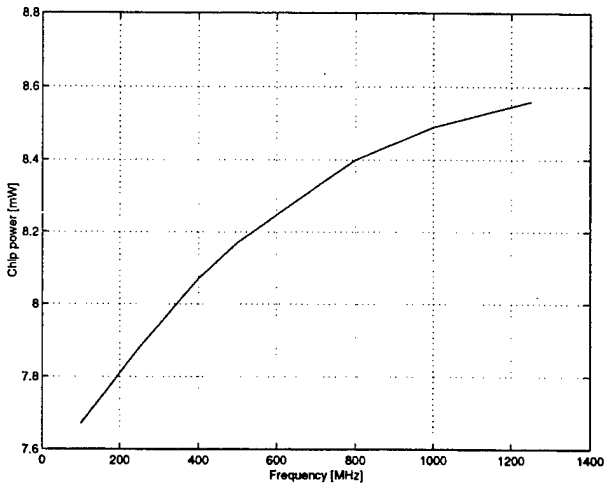


Figure 34 TDFL Chip Power vs Frequency

After the chip was thoroughly simulated for correct functionality and it was observed that the internal TDFL signals showed solid noise margins, the chip layout was submitted for fabrication through MOSIS.

D. TESTING

The testing and empirical analysis of the TDFL version of the PNSG will be performed upon completion of fabrication, which is expected in October 1997. The pin-out of the TDFL chip, shown in Appendix B, was intentionally made to be compatible with the pin-out of the DCFL chip, thus preventing the necessity of creating a separate test board. The testing will closely parallel the testing of the DCFL chip. Proper functionality will be inspected first followed by evaluation of chip power and speed characteristics.

VI. CONCLUSION

A. COMPARISON OF DCFL AND TDFL

At the time of this writing, the TDFL PNSG chips had not yet been fabricated. However, the HSpice simulations performed provide a basis for comparison between the two logic topologies. In Figure 35, an HSpice simulation plot shows the instantaneous internal chip power of the DCFL and TDFL implementations of the PNSG at 1 GHz with V_{dd} set to 2V. After the excess power related to the internal RESET being asserted for 4 ns, the average power of the DCFL chip was 40 mW versus 8.5 mW for the TDFL chip, for a power reduction of 79%. This power reduction is almost exclusively delivered by reducing the static current inherent in the DCFL gate design. The power reduction is even more dramatic when the two-phase clock generator is removed, as shown in the lowest power trace where the average power is then 3.2 mW or 92% less than the DCFL power consumption.

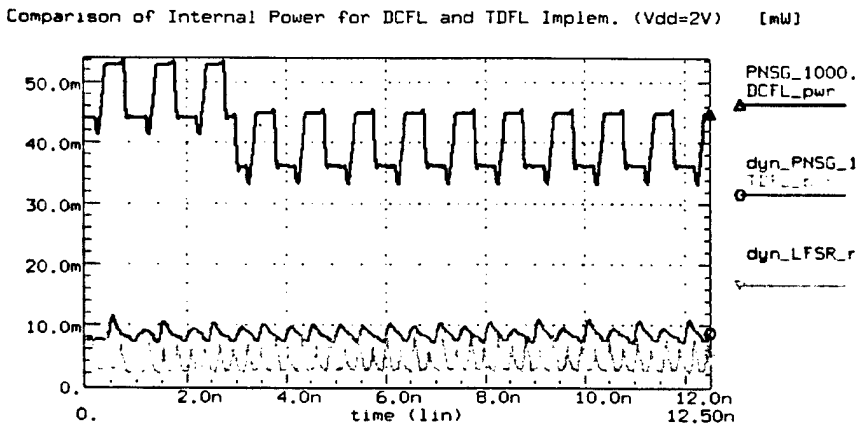


Figure 35 HSpice Plot of DCFL and TDFL PNSG Power Consumption

With regard to speed, no substantial differences were measured between the basic gates of the DCFL and TDFL designs. The two-phase clock generator of the TDFL design was the limiting factor for that chip. This was due to the asymmetry of the $\Phi 1$ and $\Phi 2$ clock signals, as previously mentioned. For this reason, the internal chip simulated successfully at up to 1.2 GHz for the TDFL design, compared to 2 GHz for the DCFL LFSR circuit.

Little effort was made to minimize layout area because the two chips designed were not particularly complex. As a result, accurately assessing the comparative layout areas of the two chips is difficult. While the non-ratioed nature of the TDFL gates allowed the use of minimum-size FETs, there were more FETs per gate. For example, in the inverter, the DCFL inverter is comprised of one EFET and one DFET compared to two EFETs and three DFETs for the TDFL inverter. However, the D flip-flop was implemented in DCFL using 22 FETs compared to only 11 FETs for the TDFL implementation. An additional layout cost of TDFL is the added area and complexity associated with routing the two clocking signals to all the TDFL gates. In general, TDFL offers layout area savings on circuits which are largely synchronous and pipelined and less if any area reduction for circuits requiring extensive logic such as an arithmetic logic unit.

One method of evaluating the comparative layout areas is to look at the total active gate area of the two designs. Using a simple C++ program shown in Appendix E, the respective HSpice files were processed to determine the sum of all gate areas in each layout. This analysis revealed that the DCFL chip (excluding pad drivers and receivers)

had a total gate area of 3712 μm^2 and the total for the TDFL chip was 2644.3 μm^2, a 28.8% reduction in total gate area. The TDFL figure represents the gate area of all FETs including the capacitance generating EFETs at the output of each gate as well as the two-phase clock generator. This comparison provides some sense for the layout savings afforded through the use of TDFL circuits.

A final point of comparison is the complexity and time involved in designing with each topology. The DCFL design was relatively straightforward and progressed smoothly. DCFL presented little in the way of challenging design considerations. The TDFL design was more challenging for several reasons. Thinking in terms of a pipelined architecture, as one must with TDFL, required some adjustment. An example of this challenge is evident in the design of the TDFL PNSG all-zero correction logic which was non-optimal at the time of fabrication. As mentioned, layout was also somewhat more challenging because of the additional routing inherent in TDFL, not to mention that the library of components had to be designed, laid out, and tested, unlike the DCFL where a library of basic gates already existed. The requirement that TDFL gates be chained in a phase-complementary manner (i.e. a $\Phi 1$ gate output cannot be a $\Phi 1$ gate input) also added to the complexity of the design.

B. IMPROVEMENTS AND FUTURE WORK

This thesis work has succeeded in producing two chip designs, one of which has been run successfully at speeds of nearly 1 GHz. Notwithstanding this success, several improvements can be made in both the DCFL and TDFL designs.

The layout of the DCFL device can be compacted somewhat. The pad ring could be compressed with the same pin-out and the internal gates could be more economically packed together. This would save layout area and reduce circuit parasitics. Chip testing would be facilitated by producing a "trigger" output. This could be accomplished by taking a NAND of Q1 through Q7 and routing it to an external driver such that the circuit triggers every time the sequence is all-high.

Because the GaAs chips run at high clock rates, it is very important that the test configuration and equipment create a minimum of additional resistance, capacitance, and inductance. The test board used in this thesis proved useful up to 1 GHz but a more refined test board would reduce high frequency noise artifacts and allow improved high frequency performance and testing. Such a refinement would involve eliminating soldering RG 174 directly to the test board by using a single chip-mounting board specifically built for use with the LDCC28 package.

The TDFL design offers several points for potential improvement. Starting at the most basic level, the inverters and NOR gates of this thesis used switching EFETs with a width of 6 μm. As previously stated, noise margins might be improved by using narrower switching EFETs, perhaps 4 μm. The capacitance-providing FET at the output of the TDFL gates should be set to the reverse-bias diode configuration to allow smaller gate sizes than those used in the chips of this thesis.

As was shown in Figure 31, it is possible to implement the 7-bit PNSG in TDFL using only five TDFL "flip-flops." Eliminating the four TDFL inverters that make up the Q6 and Q7 flip-flops would reduce layout area and power. Further, using the improved

design would result in the correction from an all-zero state occurring one cycle sooner. It would correct the erroneous state in a fraction of a cycle because it takes full advantage of the inherent pipelining in TDFL.

When the TDFL chips are tested, the present layout does not allow for isolation of the power consumed by the two-phase clock generator because it is on the same power bus as the rest of the internal circuitry. In future TDFL designs, it would be advisable to provide the clock generator its own separate power supply because its power consumption is generally a majority of the total power consumed by the inner circuitry. A clearer understanding of the power demands of TDFL is produced by this separation of supply voltages. As with the DCFL chip, the TDFL chip would benefit from having a triggering output and an improved test board.

Future testing of the fabricated chips should include a comparison of the radiation tolerance of the functionally equivalent chips. In particular, investigating the susceptibility to single event upsets of the TDFL chip in comparison to the DCFL chips would add considerably to the body of knowledge about TDFL single event effects.

C. IMPLICATIONS

The results of this thesis lead to several implications regarding GaAs design and the question of whether to use a dynamic logic topology. The speed of GaAs is well known and was clearly evident in the performance of the DCFL chips tested. Because communication systems require growing speed performance, GaAs is a logical design option. While the DCFL topology offers excellent speed performance, its power

consumption has been shown to be less than optimal. The TDFL topology investigated in this thesis offers a demonstrated solution to the power issue.

The GaAs designer must be aware of the tradeoffs inherent in these two design topologies. DCFL offers a relatively simple, high speed, higher power, option in producing an application-specific integrated circuit or even an LSI or VLSI chip. If the component to be created demands reduced power consumption and high speed performance, then GaAs TDFL offers a somewhat more complex alternative but one which provides the desired power savings over a DCFL design.

Space-based, spread-spectrum communications equipment would be improved markedly by implementing their high-speed logic needs in TDFL GaAs. The higher speed and inherent radiation tolerance of GaAs circuitry combined with the reduced power consumption of the TDFL topology make this an ideal approach. Impending testing of the fabricated TDFL PNSG chips will provide an excellent basis for a more complete comparison of the two logic topologies and thus, extend the body of knowledge on TDFL GaAs design.

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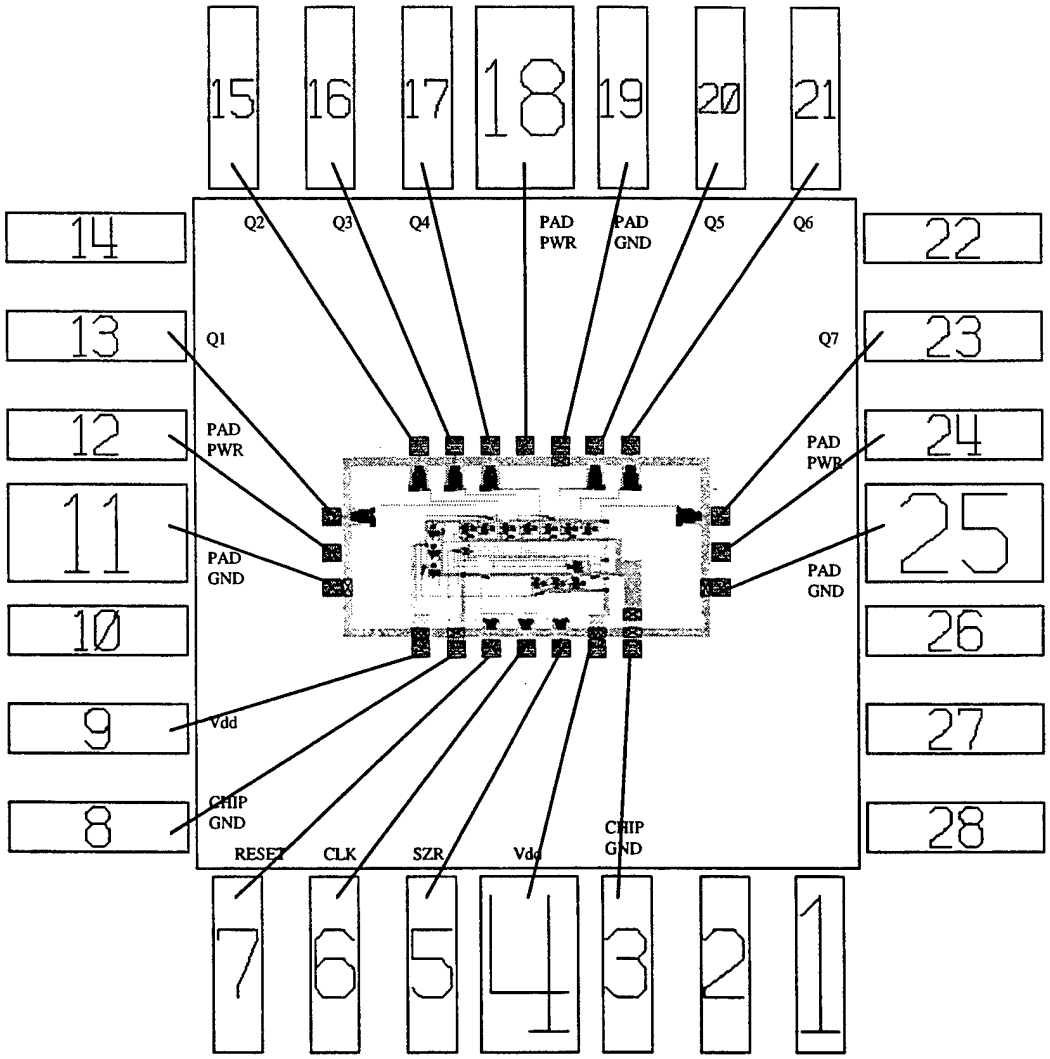
APPENDIX A. BONDING DIAGRAM FOR DCFL PNSG CHIP

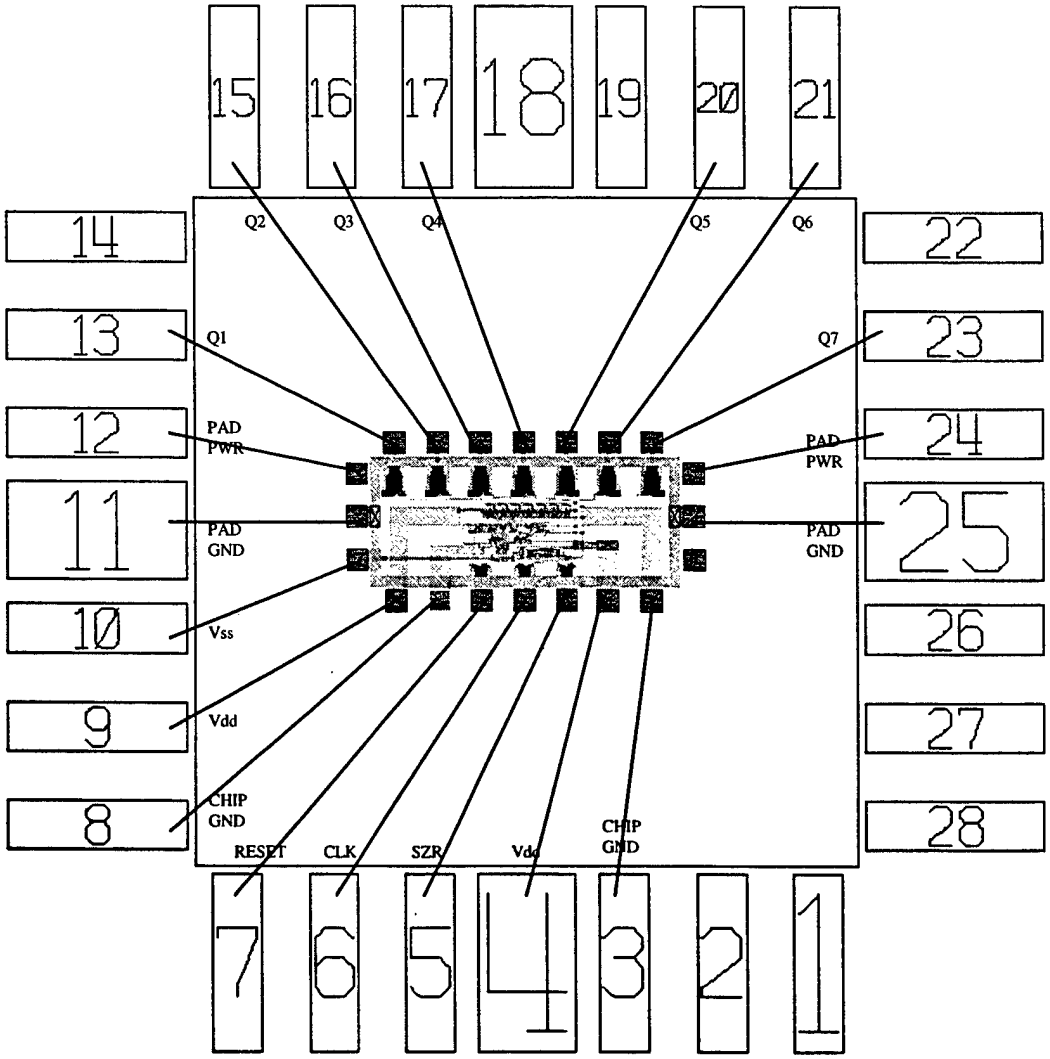


N6AAAA

50019/Fouts/PNSG

LDCC28: 20 PARTS

APPENDIX B. BONDING DIAGRAM FOR TDFL PNSG CHIP



N76UAC

52144/Fouts/DPNSG

LDCC28:

APPENDIX C. HSPICE CODE FOR DCFL PNSG SIMULATION

The following HSpice file was generated by extracting a Magic GaAs layout to an HSpice file, thus insuring an exact match between the Magic layout and the simulation.

```
** HSPICE file created to simulate DCFL PNSG Chip

** Technology: hgaas3
** include Vitesse HGaAs3 models and parameters for hspice
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect

*chip power supply
Vdd 1 0 1.5

*pad power supply
Vpadpwr 106 0 1.0
Vpadgnd 101 0 0

*CLK input at 1 GHz
* Squared wave
vCLK 252 0 pulse(0.2V 1.2V 50PS 150PS 150PS 350PS 1000PS)

*RESET
vRESET 248 0 0

*SZR input
vSZR 256 0 0.0

************************  INPUT SIGNALS  ********************
** NODE: 256 = SZR_PIN
** NODE: 252 = CLK_PIN
** NODE: 248 = RESET_PIN

*********************  Internal DCFL signals  ***************
** NODE: 138 = Q7
** NODE: 131 = Q6
** NODE: 129 = Q5
** NODE: 126 = Q4
** NODE: 125 = Q3
** NODE: 119 = Q2
** NODE: 136 = Q1

************************  OUTPUT SIGNALS  ********************
** NODE: 143 = Q7_PIN
** NODE: 105 = Q6_PIN
** NODE: 104 = Q5_PIN
** NODE: 103 = Q4_PIN
** NODE: 102 = Q3_PIN
** NODE: 100 = Q2_PIN
** NODE: 133 = Q1_PIN

************************  POWER SUPPLY  **********************
** NODE: 106 = Pad_pwr
** NODE: 101 = Pad_gnd
** NODE: 1 = Vdd
** NODE: 0 = GND

****************** Output Driver Loads **********************
R1 133 0 50
R2 100 0 50
R3 102 0 50
R4 103 0 50
R5 104 0 50
R6 105 0 50
R7 143 0 50

j0 100 101 100 0 dp1.3 l=2.0 w=50.0
j1 102 101 102 0 dp1.3 l=2.0 w=50.0
j2 103 101 103 0 dp1.3 l=2.0 w=50.0
j3 104 101 104 0 dp1.3 l=2.0 w=50.0
j4 105 101 105 0 dp1.3 l=2.0 w=50.0
j5 100 101 100 0 dp1.3 l=2.0 w=50.0
j6 102 101 102 0 dp1.3 l=2.0 w=50.0
j7 103 101 103 0 dp1.3 l=2.0 w=50.0
```

```
j8 104 101 104 0 dp1.3 l=2.0 w=50.0
j9 105 101 105 0 dp1.3 l=2.0 w=50.0
j10 106 100 106 0 dp1.3 l=2.0 w=50.0
j11 106 102 106 0 dp1.3 l=2.0 w=50.0
j12 106 103 106 0 dp1.3 l=2.0 w=50.0
j13 106 104 106 0 dp1.3 l=2.0 w=50.0
j14 106 105 106 0 dp1.3 l=2.0 w=50.0
j15 106 100 106 0 dp1.3 l=2.0 w=50.0
j16 106 102 106 0 dp1.3 l=2.0 w=50.0
j17 106 103 106 0 dp1.3 l=2.0 w=50.0
j18 106 104 106 0 dp1.3 l=2.0 w=50.0
j19 106 105 106 0 dp1.3 l=2.0 w=50.0
j20 100 107 106 0 enh.1 l=0.8 w=63.2
j21 106 107 100 0 enh.1 l=0.8 w=63.2
j22 100 107 106 0 enh.1 l=0.8 w=63.2
j23 106 107 100 0 enh.1 l=0.8 w=63.2
j24 100 107 106 0 enh.1 l=0.8 w=62.4
j25 106 107 100 0 enh.1 l=0.8 w=63.2
j26 100 107 106 0 enh.1 l=0.8 w=63.2
j27 106 107 100 0 enh.1 l=0.8 w=63.2
j28 100 107 106 0 enh.1 l=0.8 w=63.2
j29 106 107 100 0 enh.1 l=0.8 w=63.2
j30 102 108 106 0 enh.1 l=0.8 w=63.2
j31 106 108 102 0 enh.1 l=0.8 w=63.2
j32 102 108 106 0 enh.1 l=0.8 w=63.2
j33 106 108 102 0 enh.1 l=0.8 w=63.2
j34 102 108 106 0 enh.1 l=0.8 w=62.4
j35 106 108 102 0 enh.1 l=0.8 w=63.2
j36 102 108 106 0 enh.1 l=0.8 w=63.2
j37 106 108 102 0 enh.1 l=0.8 w=63.2
j38 102 108 106 0 enh.1 l=0.8 w=63.2
j39 106 108 102 0 enh.1 l=0.8 w=63.2
j40 103 109 106 0 enh.1 l=0.8 w=63.2
j41 106 109 103 0 enh.1 l=0.8 w=63.2
j42 103 109 106 0 enh.1 l=0.8 w=63.2
j43 106 109 103 0 enh.1 l=0.8 w=63.2
j44 103 109 106 0 enh.1 l=0.8 w=62.4
j45 106 109 103 0 enh.1 l=0.8 w=63.2
j46 103 109 106 0 enh.1 l=0.8 w=63.2
j47 106 109 103 0 enh.1 l=0.8 w=63.2
j48 103 109 106 0 enh.1 l=0.8 w=63.2
j49 106 109 103 0 enh.1 l=0.8 w=63.2
j50 104 110 106 0 enh.1 l=0.8 w=63.2
j51 106 110 104 0 enh.1 l=0.8 w=63.2
j52 104 110 106 0 enh.1 l=0.8 w=63.2
j53 106 110 104 0 enh.1 l=0.8 w=63.2
j54 104 110 106 0 enh.1 l=0.8 w=63.2
j55 106 110 104 0 enh.1 l=0.8 w=62.4
j56 104 110 106 0 enh.1 l=0.8 w=63.2
j57 106 110 104 0 enh.1 l=0.8 w=63.2
j58 104 110 106 0 enh.1 l=0.8 w=63.2
j59 106 110 104 0 enh.1 l=0.8 w=63.2
j60 105 111 106 0 enh.1 l=0.8 w=63.2
j61 106 111 105 0 enh.1 l=0.8 w=63.2
j62 105 111 106 0 enh.1 l=0.8 w=63.2
j63 106 111 105 0 enh.1 l=0.8 w=63.2
j64 105 111 106 0 enh.1 l=0.8 w=63.2
j65 106 111 105 0 enh.1 l=0.8 w=62.4
j66 105 111 106 0 enh.1 l=0.8 w=63.2
j67 106 111 105 0 enh.1 l=0.8 w=63.2
j68 105 111 106 0 enh.1 l=0.8 w=63.2
j69 106 111 105 0 enh.1 l=0.8 w=63.2
j70 108 112 101 0 enh.1 l=0.8 w=62.0
j71 107 113 101 0 enh.1 l=0.8 w=62.0
j72 101 113 107 0 enh.1 l=0.8 w=62.0
j73 107 113 101 0 enh.1 l=0.8 w=61.6
j74 107 114 106 0 dp1.2 l=0.8 w=23.2
j75 101 112 108 0 enh.1 l=0.8 w=62.0
j76 106 114 114 0 dp1.2 l=0.8 w=6.8
j77 106 115 113 0 dp1.2 l=0.8 w=2.0
j78 106 115 115 0 dp1.2 l=1.6 w=2.0
j79 108 112 101 0 enh.1 l=0.8 w=61.6
j80 108 116 106 0 dp1.2 l=0.8 w=23.2
j81 109 117 101 0 enh.1 l=0.8 w=62.0
j82 106 116 116 0 dp1.2 l=0.8 w=6.8
j83 101 117 109 0 enh.1 l=0.8 w=62.0
j84 106 118 112 0 dp1.2 l=0.8 w=2.0
j85 106 118 118 0 dp1.2 l=1.6 w=2.0
j86 109 117 101 0 enh.1 l=0.8 w=61.6
j87 113 119 101 0 enh.1 l=0.8 w=16.0
j88 115 119 101 0 enh.1 l=0.8 w=16.0
j89 109 120 106 0 dp1.2 l=0.8 w=23.2
j90 110 121 106 0 dp1.2 l=0.8 w=23.2
j91 106 120 120 0 dp1.2 l=0.8 w=6.8
j92 106 121 121 0 dp1.2 l=0.8 w=6.8
j93 110 122 101 0 enh.1 l=0.8 w=62.0
j94 106 123 117 0 dp1.2 l=0.8 w=2.0
j95 106 123 123 0 dp1.2 l=1.6 w=2.0
j96 106 124 124 0 dp1.2 l=1.6 w=2.0
j97 106 124 122 0 dp1.2 l=0.8 w=2.0
j98 112 125 101 0 enh.1 l=0.8 w=16.0
j99 118 125 101 0 enh.1 l=0.8 w=16.0
j100 117 126 101 0 enh.1 l=0.8 w=16.0
j101 123 126 101 0 enh.1 l=0.8 w=16.0
j102 111 127 106 0 dp1.2 l=0.8 w=23.2
j103 101 122 110 0 enh.1 l=0.8 w=62.0
j104 106 127 127 0 dp1.2 l=0.8 w=6.8
j105 111 128 101 0 enh.1 l=0.8 w=62.0
j106 110 122 101 0 enh.1 l=0.8 w=61.6
j107 124 129 101 0 enh.1 l=0.8 w=16.0
j108 122 129 101 0 enh.1 l=0.8 w=16.0
j109 106 130 130 0 dp1.2 l=1.6 w=2.0
j110 106 130 128 0 dp1.2 l=0.8 w=2.0
j111 101 128 111 0 enh.1 l=0.8 w=62.0
j112 111 128 101 0 enh.1 l=0.8 w=61.6
j113 130 131 101 0 enh.1 l=0.8 w=16.0
j114 128 131 101 0 enh.1 l=0.8 w=16.0
j115 101 112 116 0 enh.1 l=0.8 w=54.4
j116 101 117 120 0 enh.1 l=0.8 w=54.4
j117 101 122 121 0 enh.1 l=0.8 w=54.4
j118 101 113 114 0 enh.1 l=0.8 w=54.4
j119 101 128 127 0 enh.1 l=0.8 w=54.4
j120 106 132 133 0 enh.1 l=0.8 w=63.2
j121 133 101 133 0 dp1.3 l=2.0 w=50.0
j122 133 101 133 0 dp1.3 l=2.0 w=50.0
j123 106 133 106 0 dp1.3 l=2.0 w=50.0
j124 106 133 106 0 dp1.3 l=2.0 w=50.0
j125 133 132 106 0 enh.1 l=0.8 w=63.2
j126 106 132 133 0 enh.1 l=0.8 w=63.2
j127 106 134 132 0 dp1.2 l=0.8 w=23.2
j128 135 135 106 0 dp1.2 l=1.6 w=2.0
j129 101 136 135 0 enh.1 l=0.8 w=16.0
j130 137 138 101 0 enh.1 l=0.8 w=16.0
j131 106 137 137 0 dp1.2 l=1.6 w=2.0
j132 139 135 106 0 dp1.2 l=0.8 w=2.0
j133 134 134 106 0 dp1.2 l=0.8 w=6.8
j134 101 136 139 0 enh.1 l=0.8 w=16.0
j135 140 138 101 0 enh.1 l=0.8 w=16.0
j136 106 137 140 0 dp1.2 l=0.8 w=2.0
j137 133 132 106 0 enh.1 l=0.8 w=63.2
j138 106 141 141 0 dp1.2 l=0.8 w=6.8
j139 142 141 106 0 dp1.2 l=0.8 w=23.2
j140 106 142 143 0 enh.1 l=0.8 w=63.2
j141 143 142 106 0 enh.1 l=0.8 w=63.2
j142 106 142 143 0 enh.1 l=0.8 w=63.2
j143 143 142 106 0 enh.1 l=0.8 w=63.2
j144 106 132 133 0 enh.1 l=0.8 w=63.2
j145 133 132 106 0 enh.1 l=0.8 w=62.4
j146 106 132 133 0 enh.1 l=0.8 w=63.2
j147 133 132 106 0 enh.1 l=0.8 w=63.2
j148 106 132 133 0 enh.1 l=0.8 w=63.2
j149 133 132 106 0 enh.1 l=0.8 w=63.2
j150 101 139 132 0 enh.1 l=0.8 w=62.0
j151 132 139 101 0 enh.1 l=0.8 w=62.0
j152 101 139 132 0 enh.1 l=0.8 w=61.6
j153 134 139 101 0 enh.1 l=0.8 w=54.4
j154 0 144 145 0 enh.1 l=0.8 w=16.0
j155 0 144 146 0 enh.1 l=0.8 w=16.0
j156 0 144 147 0 enh.1 l=0.8 w=16.0
j157 0 144 148 0 enh.1 l=0.8 w=16.0
j158 145 145 1 0 dp1.2 l=1.6 w=2.0
j159 146 145 1 0 enh.1 l=0.8 w=16.0
j160 147 147 1 0 dp1.2 l=1.6 w=2.0
j161 148 147 1 0 enh.1 l=0.8 w=16.0
j162 149 150 0 0 enh.1 l=0.8 w=16.0
j163 0 151 149 0 enh.1 l=0.8 w=16.0
j164 150 0 0 0 enh.1 l=0.8 w=16.0
j165 149 149 1 0 dp1.2 l=1.6 w=2.0
j166 1 152 152 0 dp1.2 l=1.6 w=2.0
j167 1 151 151 0 dp1.2 l=1.6 w=2.0
```

```
j168 152 153 0 0 enh.1 l=0.8 w=16.0
j169 0 149 150 0 enh.1 l=0.8 w=16.0
j170 150 154 0 0 enh.1 l=0.8 w=16.0
j171 0 155 156 0 enh.1 l=0.8 w=16.0
j172 0 157 158 0 enh.1 l=0.8 w=16.0
j173 1 156 156 0 dp1.2 l=1.6 w=2.0
j174 0 159 160 0 enh.1 l=0.8 w=16.0
j175 1 158 158 0 dp1.2 l=1.6 w=2.0
j176 0 161 162 0 enh.1 l=0.8 w=16.0
j177 1 160 160 0 dp1.2 l=1.6 w=2.0
j178 0 163 164 0 enh.1 l=0.8 w=16.0
j179 1 162 162 0 dp1.2 l=1.6 w=2.0
j180 156 165 0 0 enh.1 l=0.8 w=16.0
j181 158 166 0 0 enh.1 l=0.8 w=16.0
j182 160 167 0 0 enh.1 l=0.8 w=16.0
j183 162 168 0 0 enh.1 l=0.8 w=16.0
j184 0 169 170 0 enh.1 l=0.8 w=16.0
j185 1 164 164 0 dp1.2 l=1.6 w=2.0
j186 0 171 172 0 enh.1 l=0.8 w=16.0
j187 1 170 170 0 dp1.2 l=1.6 w=2.0
j188 164 173 0 0 enh.1 l=0.8 w=16.0
j189 0 156 165 0 enh.1 l=0.8 w=16.0
j190 1 165 165 0 dp1.2 l=1.6 w=2.0
j191 165 146 0 0 enh.1 l=0.8 w=16.0
j192 0 158 166 0 enh.1 l=0.8 w=16.0
j193 0 174 136 0 enh.1 l=0.8 w=16.0
j194 1 166 166 0 dp1.2 l=1.6 w=2.0
j195 136 136 1 0 dp1.2 l=1.6 w=2.0
j196 150 150 1 0 dp1.2 l=1.6 w=2.0
j197 1 154 154 0 dp1.2 l=1.6 w=2.0
j198 0 151 152 0 enh.1 l=0.8 w=16.0
j199 151 152 0 0 enh.1 l=0.8 w=16.0
j200 0 175 151 0 enh.1 l=0.8 w=16.0
j201 151 0 0 0 enh.1 l=0.8 w=16.0
j202 0 151 154 0 enh.1 l=0.8 w=16.0
j203 154 175 0 0 enh.1 l=0.8 w=16.0
j204 1 153 153 0 dp1.2 l=1.6 w=2.0
j205 176 150 0 0 enh.1 l=0.8 w=16.0
j206 136 165 0 0 enh.1 l=0.8 w=16.0
j207 0 177 165 0 enh.1 l=0.8 w=16.0
j208 1 176 176 0 dp1.2 l=1.6 w=2.0
j209 0 153 154 0 enh.1 l=0.8 w=16.0
j210 153 154 0 0 enh.1 l=0.8 w=16.0
j211 0 0 153 0 enh.1 l=0.8 w=16.0
j212 153 178 0 0 enh.1 l=0.8 w=16.0
j213 179 150 0 0 enh.1 l=0.8 w=16.0
j214 1 176 179 0 enh.1 l=0.8 w=16.0
j215 0 177 174 0 enh.1 l=0.8 w=16.0
j216 174 174 1 0 dp1.2 l=1.6 w=2.0
j217 174 136 0 0 enh.1 l=0.8 w=16.0
j218 180 165 0 0 enh.1 l=0.8 w=16.0
j219 0 180 174 0 enh.1 l=0.8 w=16.0
j220 0 146 180 0 enh.1 l=0.8 w=16.0
j221 1 180 180 0 dp1.2 l=1.6 w=2.0
j222 166 146 0 0 enh.1 l=0.8 w=16.0
j223 0 160 167 0 enh.1 l=0.8 w=16.0
j224 0 181 119 0 enh.1 l=0.8 w=16.0
j225 119 119 1 0 dp1.2 l=1.6 w=2.0
j226 119 166 0 0 enh.1 l=0.8 w=16.0
j227 0 177 166 0 enh.1 l=0.8 w=16.0
j228 180 155 0 0 enh.1 l=0.8 w=16.0
j229 0 180 155 0 enh.1 l=0.8 w=16.0
j230 1 155 155 0 dp1.2 l=1.6 w=2.0
j231 155 177 0 0 enh.1 l=0.8 w=16.0
j232 0 177 181 0 enh.1 l=0.8 w=16.0
j233 181 181 1 0 dp1.2 l=1.6 w=2.0
j234 181 119 0 0 enh.1 l=0.8 w=16.0
j235 182 166 0 0 enh.1 l=0.8 w=16.0
j236 0 182 181 0 enh.1 l=0.8 w=16.0
j237 0 146 182 0 enh.1 l=0.8 w=16.0
j238 1 182 182 0 dp1.2 l=1.6 w=2.0
j239 1 167 167 0 dp1.2 l=1.6 w=2.0
j240 167 146 0 0 enh.1 l=0.8 w=16.0
j241 0 162 168 0 enh.1 l=0.8 w=16.0
j242 0 183 125 0 enh.1 l=0.8 w=16.0
j243 125 125 1 0 dp1.2 l=1.6 w=2.0
j244 125 167 0 0 enh.1 l=0.8 w=16.0
j245 0 184 167 0 enh.1 l=0.8 w=16.0
j246 182 157 0 0 enh.1 l=0.8 w=16.0
j247 0 182 157 0 enh.1 l=0.8 w=16.0
j248 1 157 157 0 dp1.2 l=1.6 w=2.0
j249 157 177 0 0 enh.1 l=0.8 w=16.0
j250 0 184 183 0 enh.1 l=0.8 w=16.0
j251 183 183 1 0 dp1.2 l=1.6 w=2.0
j252 183 125 0 0 enh.1 l=0.8 w=16.0
j253 185 167 0 0 enh.1 l=0.8 w=16.0
j254 0 185 183 0 enh.1 l=0.8 w=16.0
j255 0 146 185 0 enh.1 l=0.8 w=16.0
j256 1 185 185 0 dp1.2 l=1.6 w=2.0
j257 1 168 168 0 dp1.2 l=1.6 w=2.0
j258 168 146 0 0 enh.1 l=0.8 w=16.0
j259 1 172 172 0 dp1.2 l=1.6 w=2.0
j260 170 186 0 0 enh.1 l=0.8 w=16.0
j261 172 187 0 0 enh.1 l=0.8 w=16.0
j262 0 164 173 0 enh.1 l=0.8 w=16.0
j263 0 188 126 0 enh.1 l=0.8 w=16.0
j264 126 126 1 0 dp1.2 l=1.6 w=2.0
j265 126 168 0 0 enh.1 l=0.8 w=16.0
j266 0 184 168 0 enh.1 l=0.8 w=16.0
j267 185 159 0 0 enh.1 l=0.8 w=16.0
j268 0 185 159 0 enh.1 l=0.8 w=16.0
j269 1 159 159 0 dp1.2 l=1.6 w=2.0
j270 159 184 0 0 enh.1 l=0.8 w=16.0
j271 0 184 188 0 enh.1 l=0.8 w=16.0
j272 188 188 1 0 dp1.2 l=1.6 w=2.0
j273 188 126 0 0 enh.1 l=0.8 w=16.0
j274 189 168 0 0 enh.1 l=0.8 w=16.0
j275 0 189 188 0 enh.1 l=0.8 w=16.0
j276 0 146 189 0 enh.1 l=0.8 w=16.0
j277 1 189 189 0 dp1.2 l=1.6 w=2.0
j278 1 173 173 0 dp1.2 l=1.6 w=2.0
j279 173 148 0 0 enh.1 l=0.8 w=16.0
j280 101 140 141 0 enh.1 l=0.8 w=54.4
j281 106 142 143 0 enh.1 l=0.8 w=63.2
j282 142 140 101 0 enh.1 l=0.8 w=61.6
j283 101 140 142 0 enh.1 l=0.8 w=62.0
j284 142 140 101 0 enh.1 l=0.8 w=62.0
j285 143 142 106 0 enh.1 l=0.8 w=62.4
j286 106 142 143 0 enh.1 l=0.8 w=63.2
j287 143 142 106 0 enh.1 l=0.8 w=63.2
j288 106 142 143 0 enh.1 l=0.8 w=63.2
j289 106 143 106 0 dp1.3 l=2.0 w=50.0
j290 106 143 106 0 dp1.3 l=2.0 w=50.0
j291 143 101 143 0 dp1.3 l=2.0 w=50.0
j292 143 101 143 0 dp1.3 l=2.0 w=50.0
j293 143 142 106 0 enh.1 l=0.8 w=63.2
j294 0 170 186 0 enh.1 l=0.8 w=16.0
j295 0 190 129 0 enh.1 l=0.8 w=16.0
j296 129 129 1 0 dp1.2 l=1.6 w=2.0
j297 129 173 0 0 enh.1 l=0.8 w=16.0
j298 0 191 173 0 enh.1 l=0.8 w=16.0
j299 189 161 0 0 enh.1 l=0.8 w=16.0
j300 0 189 161 0 enh.1 l=0.8 w=16.0
j301 1 161 161 0 dp1.2 l=1.6 w=2.0
j302 0 192 155 0 enh.1 l=0.8 w=16.0
j303 0 136 157 0 enh.1 l=0.8 w=16.0
j304 161 184 0 0 enh.1 l=0.8 w=16.0
j305 0 191 190 0 enh.1 l=0.8 w=16.0
j306 190 190 1 0 dp1.2 l=1.6 w=2.0
j307 190 129 0 0 enh.1 l=0.8 w=16.0
j308 193 173 0 0 enh.1 l=0.8 w=16.0
j309 0 193 190 0 enh.1 l=0.8 w=16.0
j310 0 148 193 0 enh.1 l=0.8 w=16.0
j311 1 193 193 0 dp1.2 l=1.6 w=2.0
j312 1 186 186 0 dp1.2 l=1.6 w=2.0
j313 186 148 0 0 enh.1 l=0.8 w=16.0
j314 0 172 187 0 enh.1 l=0.8 w=16.0
j315 0 194 131 0 enh.1 l=0.8 w=16.0
j316 131 131 1 0 dp1.2 l=1.6 w=2.0
j317 131 186 0 0 enh.1 l=0.8 w=16.0
j318 0 191 186 0 enh.1 l=0.8 w=16.0
j319 193 163 0 0 enh.1 l=0.8 w=16.0
j320 0 193 163 0 enh.1 l=0.8 w=16.0
j321 1 163 163 0 dp1.2 l=1.6 w=2.0
j322 163 191 0 0 enh.1 l=0.8 w=16.0
j323 0 191 194 0 enh.1 l=0.8 w=16.0
j324 194 194 1 0 dp1.2 l=1.6 w=2.0
j325 194 131 0 0 enh.1 l=0.8 w=16.0
j326 195 186 0 0 enh.1 l=0.8 w=16.0
j327 0 195 194 0 enh.1 l=0.8 w=16.0
```

```
j328 0 148 195 0 enh.1 l=0.8 w=16.0
j329 1 195 195 0 dp1.2 l=1.6 w=2.0
j330 1 187 187 0 dp1.2 l=1.6 w=2.0
j331 187 148 0 0 enh.1 l=0.8 w=16.0
j332 0 196 138 0 enh.1 l=0.8 w=16.0
j333 138 138 1 0 dp1.2 l=1.6 w=2.0
j334 138 187 0 0 enh.1 l=0.8 w=16.0
j335 0 197 187 0 enh.1 l=0.8 w=16.0
j336 195 169 0 0 enh.1 l=0.8 w=16.0
j337 0 195 169 0 enh.1 l=0.8 w=16.0
j338 1 169 169 0 dp1.2 l=1.6 w=2.0
j339 0 119 159 0 enh.1 l=0.8 w=16.0
j340 0 125 161 0 enh.1 l=0.8 w=16.0
j341 169 191 0 0 enh.1 l=0.8 w=16.0
j342 0 197 196 0 enh.1 l=0.8 w=16.0
j343 196 196 1 0 dp1.2 l=1.6 w=2.0
j344 196 138 0 0 enh.1 l=0.8 w=16.0
j345 198 187 0 0 enh.1 l=0.8 w=16.0
j346 0 198 196 0 enh.1 l=0.8 w=16.0
j347 0 148 198 0 enh.1 l=0.8 w=16.0
j348 1 198 198 0 dp1.2 l=1.6 w=2.0
j349 198 171 0 0 enh.1 l=0.8 w=16.0
j350 0 198 171 0 enh.1 l=0.8 w=16.0
j351 1 171 171 0 dp1.2 l=1.6 w=2.0
j352 171 197 0 0 enh.1 l=0.8 w=16.0
j353 0 126 163 0 enh.1 l=0.8 w=16.0
j354 0 129 169 0 enh.1 l=0.8 w=16.0
j355 0 131 171 0 enh.1 l=0.8 w=16.0
j356 1 199 199 0 dp1.2 l=1.6 w=2.0
j357 1 199 177 0 enh.1 l=0.8 w=16.0
j358 1 200 200 0 dp1.2 l=1.6 w=2.0
j359 1 200 184 0 enh.1 l=0.8 w=16.0
j360 199 179 0 0 enh.1 l=0.8 w=16.0
j361 177 179 0 0 enh.1 l=0.8 w=16.0
j362 1 201 201 0 dp1.2 l=1.6 w=2.0
j363 1 201 191 0 enh.1 l=0.8 w=16.0
j364 200 179 0 0 enh.1 l=0.8 w=16.0
j365 184 179 0 0 enh.1 l=0.8 w=16.0
j366 1 202 202 0 dp1.2 l=1.6 w=2.0
j367 1 202 197 0 enh.1 l=0.8 w=16.0
j368 201 179 0 0 enh.1 l=0.8 w=16.0
j369 191 179 0 0 enh.1 l=0.8 w=16.0
j370 202 179 0 0 enh.1 l=0.8 w=16.0
j371 197 179 0 0 enh.1 l=0.8 w=16.0
j372 178 203 0 0 enh.1 l=0.8 w=16.0
j373 0 204 178 0 enh.1 l=0.8 w=16.0
j374 203 0 0 0 enh.1 l=0.8 w=16.0
j375 178 178 1 0 dp1.2 l=1.6 w=2.0
j376 1 205 205 0 dp1.2 l=1.6 w=2.0
j377 1 204 204 0 dp1.2 l=1.6 w=2.0
j378 205 206 0 0 enh.1 l=0.8 w=16.0
j379 0 178 203 0 enh.1 l=0.8 w=16.0
j380 203 207 0 0 enh.1 l=0.8 w=16.0
j381 203 203 1 0 dp1.2 l=1.6 w=2.0
j382 208 136 0 0 enh.1 l=0.8 w=16.0
j383 0 119 208 0 enh.1 l=0.8 w=16.0
j384 1 207 207 0 dp1.2 l=1.6 w=2.0
j385 0 204 205 0 enh.1 l=0.8 w=16.0
j386 204 205 0 0 enh.1 l=0.8 w=16.0
j387 0 175 204 0 enh.1 l=0.8 w=16.0
j388 204 0 0 0 enh.1 l=0.8 w=16.0
j389 0 204 207 0 enh.1 l=0.8 w=16.0
j390 207 175 0 0 enh.1 l=0.8 w=16.0
j391 1 206 206 0 dp1.2 l=1.6 w=2.0
j392 0 206 207 0 enh.1 l=0.8 w=16.0
j393 206 207 0 0 enh.1 l=0.8 w=16.0
j394 0 209 210 0 enh.1 l=0.8 w=16.0
j395 0 208 210 0 enh.1 l=0.8 w=16.0
j396 0 0 206 0 enh.1 l=0.8 w=16.0
j397 206 211 0 0 enh.1 l=0.8 w=16.0
j398 208 125 0 0 enh.1 l=0.8 w=16.0
j399 210 210 1 0 dp1.2 l=1.6 w=2.0
j400 0 126 208 0 enh.1 l=0.8 w=16.0
j401 208 208 1 0 dp1.2 l=1.6 w=2.0
j402 208 129 0 0 enh.1 l=0.8 w=16.0
j403 0 131 208 0 enh.1 l=0.8 w=16.0
j404 208 138 0 0 enh.1 l=0.8 w=16.0
j405 212 194 0 0 enh.1 l=0.8 w=16.0
j406 0 196 212 0 enh.1 l=0.8 w=16.0
j407 212 212 1 0 dp1.2 l=1.6 w=2.0
j408 212 213 0 0 enh.1 l=0.8 w=16.0
j409 175 144 0 0 enh.1 l=0.8 w=16.0
j410 1 214 175 0 enh.1 l=0.8 w=16.0
j411 211 215 0 0 enh.1 l=0.8 w=16.0
j412 0 216 211 0 enh.1 l=0.8 w=16.0
j413 215 0 0 0 enh.1 l=0.8 w=16.0
j414 211 211 1 0 dp1.2 l=1.6 w=2.0
j415 214 144 0 0 enh.1 l=0.8 w=16.0
j416 1 214 214 0 dp1.2 l=1.6 w=2.0
j417 1 217 217 0 dp1.2 l=1.6 w=2.0
j418 1 216 216 0 dp1.2 l=1.6 w=2.0
j419 217 218 0 0 enh.1 l=0.8 w=16.0
j420 0 211 215 0 enh.1 l=0.8 w=16.0
j421 215 219 0 0 enh.1 l=0.8 w=16.0
j422 0 194 220 0 enh.1 l=0.8 w=16.0
j423 220 220 1 0 dp1.2 l=1.6 w=2.0
j424 220 138 0 0 enh.1 l=0.8 w=16.0
j425 0 212 192 0 enh.1 l=0.8 w=16.0
j426 192 192 1 0 dp1.2 l=1.6 w=2.0
j427 0 221 220 0 enh.1 l=0.8 w=16.0
j428 192 220 0 0 enh.1 l=0.8 w=16.0
j429 215 215 1 0 dp1.2 l=1.6 w=2.0
j430 0 222 192 0 enh.1 l=0.8 w=16.0
j431 222 131 0 0 enh.1 l=0.8 w=16.0
j432 192 223 0 0 enh.1 l=0.8 w=16.0
j433 1 219 219 0 dp1.2 l=1.6 w=2.0
j434 0 216 217 0 enh.1 l=0.8 w=16.0
j435 216 217 0 0 enh.1 l=0.8 w=16.0
j436 0 175 216 0 enh.1 l=0.8 w=16.0
j437 216 0 0 0 enh.1 l=0.8 w=16.0
j438 0 216 219 0 enh.1 l=0.8 w=16.0
j439 219 175 0 0 enh.1 l=0.8 w=16.0
j440 1 218 218 0 dp1.2 l=1.6 w=2.0
j441 0 196 222 0 enh.1 l=0.8 w=16.0
j442 222 222 1 0 dp1.2 l=1.6 w=2.0
j443 222 221 0 0 enh.1 l=0.8 w=16.0
j444 0 218 219 0 enh.1 l=0.8 w=16.0
j445 218 219 0 0 enh.1 l=0.8 w=16.0
j446 0 131 223 0 enh.1 l=0.8 w=16.0
j447 0 0 218 0 enh.1 l=0.8 w=16.0
j448 218 210 0 0 enh.1 l=0.8 w=16.0
j449 223 223 1 0 dp1.2 l=1.6 w=2.0
j450 223 138 0 0 enh.1 l=0.8 w=16.0
j451 0 213 223 0 enh.1 l=0.8 w=16.0
j452 0 224 225 0 enh.1 l=0.8 w=16.0
j453 0 224 144 0 enh.1 l=0.8 w=16.0
j454 0 213 221 0 enh.1 l=0.8 w=16.0
j455 0 213 226 0 enh.1 l=0.8 w=16.0
j456 225 225 1 0 dp1.2 l=1.6 w=2.0
j457 144 225 1 0 enh.1 l=0.8 w=16.0
j458 227 228 0 0 enh.1 l=0.8 w=16.0
j459 221 226 1 0 enh.1 l=0.8 w=16.0
j460 229 230 0 0 enh.1 l=0.8 w=16.0
j461 231 232 0 0 enh.1 l=0.8 w=16.0
j462 226 226 1 0 dp1.2 l=1.6 w=2.0
j463 0 0 227 0 enh.1 l=0.8 w=16.0
j464 0 0 229 0 enh.1 l=0.8 w=16.0
j465 1 227 227 0 dp1.2 l=1.6 w=2.0
j466 227 233 0 0 enh.1 l=0.8 w=16.0
j467 0 227 233 0 enh.1 l=0.8 w=16.0
j468 1 233 233 0 dp1.2 l=1.6 w=2.0
j469 233 234 0 0 enh.1 l=0.8 w=16.0
j470 235 233 0 0 enh.1 l=0.8 w=16.0
j471 0 236 233 0 enh.1 l=0.8 w=16.0
j472 0 230 235 0 enh.1 l=0.8 w=16.0
j473 235 235 1 0 dp1.2 l=1.6 w=2.0
j474 235 0 0 0 enh.1 l=0.8 w=16.0
j475 236 0 0 0 enh.1 l=0.8 w=16.0
j476 0 236 230 0 enh.1 l=0.8 w=16.0
j477 0 234 236 0 enh.1 l=0.8 w=16.0
j478 230 230 1 0 dp1.2 l=1.6 w=2.0
j479 1 236 236 0 dp1.2 l=1.6 w=2.0
j480 0 0 231 0 enh.1 l=0.8 w=16.0
j481 1 229 229 0 dp1.2 l=1.6 w=2.0
j482 229 237 0 0 enh.1 l=0.8 w=16.0
j483 0 229 237 0 enh.1 l=0.8 w=16.0
j484 1 237 237 0 dp1.2 l=1.6 w=2.0
j485 237 234 0 0 enh.1 l=0.8 w=16.0
j486 238 237 0 0 enh.1 l=0.8 w=16.0
j487 0 239 237 0 enh.1 l=0.8 w=16.0
```

```
j488 0 232 238 0 enh.1 l=0.8 w=16.0
j490 238 0 0 0 enh.1 l=0.8 w=16.0
j491 239 0 0 0 enh.1 l=0.8 w=16.0
j492 230 235 0 0 enh.1 l=0.8 w=16.0
j493 0 239 232 0 enh.1 l=0.8 w=16.0
j494 0 234 239 0 enh.1 l=0.8 w=16.0
j495 236 240 0 0 enh.1 l=0.8 w=16.0
j496 232 232 1 0 dp1.2 l=1.6 w=2.0
j497 1 239 239 0 dp1.2 l=1.6 w=2.0
j498 1 231 231 0 dp1.2 l=1.6 w=2.0
j499 231 241 0 0 enh.1 l=0.8 w=16.0
j500 0 231 241 0 enh.1 l=0.8 w=16.0
j501 1 241 241 0 dp1.2 l=1.6 w=2.0
j502 241 234 0 0 enh.1 l=0.8 w=16.0
j503 242 241 0 0 enh.1 l=0.8 w=16.0
j504 0 243 241 0 enh.1 l=0.8 w=16.0
j505 0 213 242 0 enh.1 l=0.8 w=16.0
j506 242 242 1 0 dp1.2 l=1.6 w=2.0
j507 242 0 0 0 enh.1 l=0.8 w=16.0
j508 243 0 0 0 enh.1 l=0.8 w=16.0
j509 232 238 0 0 enh.1 l=0.8 w=16.0
j510 0 243 213 0 enh.1 l=0.8 w=16.0
j511 0 234 243 0 enh.1 l=0.8 w=16.0
j512 239 244 0 0 enh.1 l=0.8 w=16.0
j513 213 213 1 0 dp1.2 l=1.6 w=2.0
j514 1 243 243 0 dp1.2 l=1.6 w=2.0
j515 213 242 0 0 enh.1 l=0.8 w=16.0
j516 243 245 0 0 enh.1 l=0.8 w=16.0
j517 0 236 240 0 enh.1 l=0.8 w=16.0
j518 0 239 244 0 enh.1 l=0.8 w=16.0
j519 0 243 245 0 enh.1 l=0.8 w=16.0
j520 1 240 240 0 dp1.2 l=1.6 w=2.0
j521 240 227 0 0 enh.1 l=0.8 w=16.0
j522 1 244 244 0 dp1.2 l=1.6 w=2.0
j523 244 229 0 0 enh.1 l=0.8 w=16.0
j524 1 245 245 0 dp1.2 l=1.6 w=2.0
j525 245 231 0 0 enh.1 l=0.8 w=16.0
j526 1 246 246 0 dp1.2 l=1.6 w=2.0
j527 1 246 234 0 enh.1 l=0.8 w=16.0
j489 238 238 1 0 dp1.2 l=1.6 w=2.0
j528 246 144 0 0 enh.1 l=0.8 w=16.0
j529 234 144 0 0 enh.1 l=0.8 w=16.0
j530 106 247 209 0 enh.1 l=0.8 w=16.0
j531 106 247 247 0 dp1.2 l=1.6 w=2.0
j532 106 248 249 0 enh.1 l=0.8 w=16.0
j533 106 250 250 0 dp1.2 l=1.6 w=2.0
j534 106 251 224 0 enh.1 l=0.8 w=16.0
j535 106 251 251 0 dp1.2 l=1.6 w=2.0
j536 106 252 253 0 enh.1 l=0.8 w=16.0
j537 209 250 101 0 enh.1 l=0.8 w=16.0
j538 247 250 101 0 enh.1 l=0.8 w=16.0
j539 249 101 101 0 dp1.2 l=1.6 w=2.0
j540 106 254 254 0 dp1.2 l=1.6 w=2.0
j541 106 255 228 0 enh.1 l=0.8 w=16.0
j542 106 255 255 0 dp1.2 l=1.6 w=2.0
j543 106 256 257 0 enh.1 l=0.8 w=16.0
j544 224 254 101 0 enh.1 l=0.8 w=16.0
j545 251 254 101 0 enh.1 l=0.8 w=16.0
j546 250 249 101 0 enh.1 l=0.8 w=16.0
j547 253 101 101 0 dp1.2 l=1.6 w=2.0
j548 106 258 258 0 dp1.2 l=1.6 w=2.0
j549 254 253 101 0 enh.1 l=0.8 w=16.0
j550 228 258 101 0 enh.1 l=0.8 w=16.0
j551 255 258 101 0 enh.1 l=0.8 w=16.0
j552 257 101 101 0 dp1.2 l=1.6 w=2.0
j553 258 257 101 0 enh.1 l=0.8 w=16.0
j554 106 248 106 0 dp1.3 l=2.0 w=50.0
j555 106 252 106 0 dp1.3 l=2.0 w=50.0
j556 106 256 106 0 dp1.3 l=2.0 w=50.0
j557 106 248 106 0 dp1.3 l=2.0 w=50.0
j558 106 252 106 0 dp1.3 l=2.0 w=50.0
j559 106 256 106 0 dp1.3 l=2.0 w=50.0
j560 248 101 248 0 dp1.3 l=2.0 w=50.0
j561 252 101 252 0 dp1.3 l=2.0 w=50.0
j562 256 101 256 0 dp1.3 l=2.0 w=50.0
j563 248 101 248 0 dp1.3 l=2.0 w=50.0
j564 252 101 252 0 dp1.3 l=2.0 w=50.0

*analysis parameters
.options scale=1E-06 post
.tran 10ps 12500ps
.MEAS avg_power avg power
.MEAS max_power max power
.MEAS rms_power rms power
.MEAS TRAN Avg_P_VDD AVG P(Vdd) FROM=0.0ns TO=10ns
.MEAS TRAN Avg_P_PAD AVG P(Vpadpwr) FROM=0.0ns TO=10ns
.end
```

APPENDIX D. HSPICE CODE FOR TDFL PNSG SIMULATION

The following HSpice file was generated by extracting a Magic GaAs layout to an HSpice file, thus insuring an exact match between the Magic layout and the simulation.

```
**  HSPICE file created for simulation of TDFL PNSG

** Technology: hgaas3
** include Vitesse HGaAs3 models and parameters for hspice
.protect
.include '/tools3/cad/meta/h92/parts/vitesse/hgaas3.models'
.lib '/tools3/cad/meta/h92/parts/vitesse/hgaas3.corners' typical
.unprotect

* Chip power supply
Vdd 1 0 2.0
Vss 263 0 -2.0

* Pad power and gnd
Vpad_pwr 108 0 2.0
Vpad_gnd 101 0 0

*CLK input at 1 GHz
vCLK 284 0 pulse(0.2V 1.2V 50PS 150PS 150PS 350PS 1000PS)

*RESET
vRESET 280 0 0

*SZR input
vSZR 288 0 0

************************  INPUT SIGNALS  ********************
** NODE: 288 = SZR_PIN
** NODE: 284 = CLK_PIN
** NODE: 280 = RESET_PIN

*********************  Internal TDFL signals  ***************
** NODE: 164 = Q7
** NODE: 162 = Q6
** NODE: 160 = Q5
** NODE: 158 = Q4
** NODE: 156 = Q3
** NODE: 154 = Q2
** NODE: 151 = Q1

************************  OUTPUT SIGNALS  *******************
** NODE: 107 = Q7_PIN
** NODE: 106 = Q6_PIN
** NODE: 105 = Q5_PIN
** NODE: 104 = Q4_PIN
** NODE: 103 = Q3_PIN
** NODE: 102 = Q2_PIN
** NODE: 100 = Q1_PIN

********  Internally generated 2-phase clock  *************
** NODE: 152 = PHI_1
** NODE: 167 = PHI_2

************************  POWER SUPPLY  *********************
** NODE: 108 = Pad_pwr
** NODE: 101 = Pad_gnd
** NODE: 1   = Vdd
** NODE: 0   = GND
** NODE: 263 = Vss

***************** Output Driver Loads ***********************
R1 100 0 50
R2 102 0 50
R3 103 0 50
R4 104 0 50
R5 105 0 50
R6 106 0 50
R7 107 0 50
```

```
j0 100 101 100 0 dp1.3 l=2.0 w=50.0
j1 102 101 102 0 dp1.3 l=2.0 w=50.0
j2 103 101 103 0 dp1.3 l=2.0 w=50.0
j3 104 101 104 0 dp1.3 l=2.0 w=50.0
j4 105 101 105 0 dp1.3 l=2.0 w=50.0
j5 106 101 106 0 dp1.3 l=2.0 w=50.0
j6 107 101 107 0 dp1.3 l=2.0 w=50.0
j7 100 101 100 0 dp1.3 l=2.0 w=50.0
j8 102 101 102 0 dp1.3 l=2.0 w=50.0
j9 103 101 103 0 dp1.3 l=2.0 w=50.0
j10 104 101 104 0 dp1.3 l=2.0 w=50.0
j11 105 101 105 0 dp1.3 l=2.0 w=50.0
j12 106 101 106 0 dp1.3 l=2.0 w=50.0
j13 107 101 107 0 dp1.3 l=2.0 w=50.0
j14 108 100 108 0 dp1.3 l=2.0 w=50.0
j15 108 102 108 0 dp1.3 l=2.0 w=50.0
j16 108 103 108 0 dp1.3 l=2.0 w=50.0
j17 108 104 108 0 dp1.3 l=2.0 w=50.0
j18 108 105 108 0 dp1.3 l=2.0 w=50.0
j19 108 106 108 0 dp1.3 l=2.0 w=50.0
j20 108 107 108 0 dp1.3 l=2.0 w=50.0
j21 108 100 108 0 dp1.3 l=2.0 w=50.0
j22 108 102 108 0 dp1.3 l=2.0 w=50.0
j23 108 103 108 0 dp1.3 l=2.0 w=50.0
j24 108 104 108 0 dp1.3 l=2.0 w=50.0
j25 108 105 108 0 dp1.3 l=2.0 w=50.0
j26 108 106 108 0 dp1.3 l=2.0 w=50.0
j27 108 107 108 0 dp1.3 l=2.0 w=50.0
j28 100 109 108 0 enh.1 l=0.8 w=63.2
j29 108 109 100 0 enh.1 l=0.8 w=63.2
j30 100 109 108 0 enh.1 l=0.8 w=63.2
j31 108 109 100 0 enh.1 l=0.8 w=63.2
j32 100 109 108 0 enh.1 l=0.8 w=62.4
j33 108 109 100 0 enh.1 l=0.8 w=63.2
j34 100 109 108 0 enh.1 l=0.8 w=63.2
j35 108 109 100 0 enh.1 l=0.8 w=63.2
j36 100 109 108 0 enh.1 l=0.8 w=63.2
j37 108 109 100 0 enh.1 l=0.8 w=63.2
j38 102 110 108 0 enh.1 l=0.8 w=63.2
j39 108 110 102 0 enh.1 l=0.8 w=63.2
j40 102 110 108 0 enh.1 l=0.8 w=63.2
j41 108 110 102 0 enh.1 l=0.8 w=63.2
j42 102 110 108 0 enh.1 l=0.8 w=62.4
j43 108 110 102 0 enh.1 l=0.8 w=63.2
j44 102 110 108 0 enh.1 l=0.8 w=63.2
j45 108 110 102 0 enh.1 l=0.8 w=63.2
j46 102 110 108 0 enh.1 l=0.8 w=63.2
j47 108 110 102 0 enh.1 l=0.8 w=63.2
j48 103 111 108 0 enh.1 l=0.8 w=63.2
j49 108 111 103 0 enh.1 l=0.8 w=63.2
j50 103 111 108 0 enh.1 l=0.8 w=63.2
j51 108 111 103 0 enh.1 l=0.8 w=63.2
j52 103 111 108 0 enh.1 l=0.8 w=62.4
j53 108 111 103 0 enh.1 l=0.8 w=63.2
j54 103 111 108 0 enh.1 l=0.8 w=63.2
j55 108 111 103 0 enh.1 l=0.8 w=63.2
j56 103 111 108 0 enh.1 l=0.8 w=63.2
j57 108 111 103 0 enh.1 l=0.8 w=63.2
j58 104 112 108 0 enh.1 l=0.8 w=63.2
j59 108 112 104 0 enh.1 l=0.8 w=63.2
j60 104 112 108 0 enh.1 l=0.8 w=63.2
j61 108 112 104 0 enh.1 l=0.8 w=63.2
j62 104 112 108 0 enh.1 l=0.8 w=62.4
j63 108 112 104 0 enh.1 l=0.8 w=63.2
j64 104 112 108 0 enh.1 l=0.8 w=63.2
j65 108 112 104 0 enh.1 l=0.8 w=63.2
j66 104 112 108 0 enh.1 l=0.8 w=63.2
j67 108 112 104 0 enh.1 l=0.8 w=63.2
j68 105 113 108 0 enh.1 l=0.8 w=63.2
j69 108 113 105 0 enh.1 l=0.8 w=63.2
j70 105 113 108 0 enh.1 l=0.8 w=63.2
j71 108 113 105 0 enh.1 l=0.8 w=63.2
j72 105 113 108 0 enh.1 l=0.8 w=63.2
j73 108 113 105 0 enh.1 l=0.8 w=62.4
j74 105 113 108 0 enh.1 l=0.8 w=63.2
j75 108 113 105 0 enh.1 l=0.8 w=63.2
j76 105 113 108 0 enh.1 l=0.8 w=63.2
j77 108 113 105 0 enh.1 l=0.8 w=63.2
j78 106 114 108 0 enh.1 l=0.8 w=63.2
j79 108 114 106 0 enh.1 l=0.8 w=63.2
j80 106 114 108 0 enh.1 l=0.8 w=63.2
j81 108 114 106 0 enh.1 l=0.8 w=63.2
j82 106 114 108 0 enh.1 l=0.8 w=63.2
j83 108 114 106 0 enh.1 l=0.8 w=62.4
j84 106 114 108 0 enh.1 l=0.8 w=63.2
j85 108 114 106 0 enh.1 l=0.8 w=63.2
j86 106 114 108 0 enh.1 l=0.8 w=63.2
j87 108 114 106 0 enh.1 l=0.8 w=63.2
j88 107 115 108 0 enh.1 l=0.8 w=63.2
j89 108 115 107 0 enh.1 l=0.8 w=63.2
j90 107 115 108 0 enh.1 l=0.8 w=63.2
j91 108 115 107 0 enh.1 l=0.8 w=63.2
j92 107 115 108 0 enh.1 l=0.8 w=63.2
j93 108 115 107 0 enh.1 l=0.8 w=62.4
j94 107 115 108 0 enh.1 l=0.8 w=63.2
j95 108 115 107 0 enh.1 l=0.8 w=63.2
j96 107 115 108 0 enh.1 l=0.8 w=63.2
j97 108 115 107 0 enh.1 l=0.8 w=63.2
j98 110 116 101 0 enh.1 l=0.8 w=62.0
j99 109 117 101 0 enh.1 l=0.8 w=62.0
j100 101 117 109 0 enh.1 l=0.8 w=62.0
j101 109 117 101 0 enh.1 l=0.8 w=61.6
j102 109 118 108 0 dp1.1 l=0.8 w=23.2
j103 101 116 110 0 enh.1 l=0.8 w=62.0
j104 108 118 118 0 dp1.1 l=0.8 w=6.8
j105 108 119 117 0 dp1.1 l=0.8 w=2.0
j106 108 119 119 0 dp1.2 l=1.6 w=2.0
j107 110 116 101 0 enh.1 l=0.8 w=61.6
j108 110 120 108 0 dp1.1 l=0.8 w=23.2
j109 111 121 101 0 enh.1 l=0.8 w=62.0
j110 108 120 120 0 dp1.1 l=0.8 w=6.8
j111 101 121 111 0 enh.1 l=0.8 w=62.0
j112 108 122 116 0 dp1.1 l=0.8 w=2.0
j113 108 122 122 0 dp1.2 l=1.6 w=2.0
j114 111 121 101 0 enh.1 l=0.8 w=61.6
j115 117 123 101 0 enh.1 l=0.8 w=16.0
j116 119 123 101 0 enh.1 l=0.8 w=16.0
j117 111 124 108 0 dp1.1 l=0.8 w=23.2
j118 112 125 101 0 enh.1 l=0.8 w=62.0
j119 108 124 124 0 dp1.1 l=0.8 w=6.8
j120 101 125 112 0 enh.1 l=0.8 w=62.0
j121 108 126 121 0 dp1.1 l=0.8 w=2.0
j122 108 126 126 0 dp1.2 l=1.6 w=2.0
j123 112 125 101 0 enh.1 l=0.8 w=61.6
j124 116 127 101 0 enh.1 l=0.8 w=16.0
j125 122 127 101 0 enh.1 l=0.8 w=16.0
j126 112 128 108 0 dp1.1 l=0.8 w=23.2
j127 113 129 108 0 dp1.1 l=0.8 w=23.2
j128 108 128 128 0 dp1.1 l=0.8 w=6.8
j129 108 129 129 0 dp1.1 l=0.8 w=6.8
j130 113 130 101 0 enh.1 l=0.8 w=62.0
j131 108 131 125 0 dp1.1 l=0.8 w=2.0
j132 108 131 131 0 dp1.2 l=1.6 w=2.0
j133 108 132 132 0 dp1.2 l=1.6 w=2.0
j134 108 132 130 0 dp1.1 l=0.8 w=2.0
j135 121 133 101 0 enh.1 l=0.8 w=16.0
j136 126 133 101 0 enh.1 l=0.8 w=16.0
j137 125 134 101 0 enh.1 l=0.8 w=16.0
j138 131 134 101 0 enh.1 l=0.8 w=16.0
j139 114 135 108 0 dp1.1 l=0.8 w=23.2
j140 101 130 113 0 enh.1 l=0.8 w=62.0
j141 108 135 135 0 dp1.1 l=0.8 w=6.8
j142 114 136 101 0 enh.1 l=0.8 w=62.0
j143 113 130 101 0 enh.1 l=0.8 w=61.6
j144 108 137 137 0 dp1.2 l=1.6 w=2.0
j145 108 137 136 0 dp1.1 l=0.8 w=2.0
j146 132 138 101 0 enh.1 l=0.8 w=16.0
j147 130 138 101 0 enh.1 l=0.8 w=16.0
j148 115 139 108 0 dp1.1 l=0.8 w=23.2
j149 101 136 114 0 enh.1 l=0.8 w=62.0
j150 108 139 139 0 dp1.1 l=0.8 w=6.8
j151 115 140 101 0 enh.1 l=0.8 w=62.0
j152 114 136 101 0 enh.1 l=0.8 w=61.6
j153 137 141 101 0 enh.1 l=0.8 w=16.0
j154 136 141 101 0 enh.1 l=0.8 w=16.0
j155 101 116 120 0 enh.1 l=0.8 w=54.4
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j156 101 121 124 0 enh.1 l=0.8 w=54.4
j157 101 125 128 0 enh.1 l=0.8 w=54.4
j158 101 130 129 0 enh.1 l=0.8 w=54.4
j159 108 142 142 0 dp1.2 l=1.6 w=2.0
j160 108 142 140 0 dp1.1 l=0.8 w=2.0
j161 101 140 115 0 enh.1 l=0.8 w=62.0
j162 115 140 101 0 enh.1 l=0.8 w=61.6
j163 142 143 101 0 enh.1 l=0.8 w=16.0
j164 140 143 101 0 enh.1 l=0.8 w=16.0
j165 101 117 118 0 enh.1 l=0.8 w=54.4
j166 101 136 135 0 enh.1 l=0.8 w=54.4
j167 101 140 139 0 enh.1 l=0.8 w=54.4
j168 1 123 123 0 dp1.2 l=2.8 w=2.0
j169 1 144 144 0 dp1.2 l=2.8 w=2.0
j170 1 127 127 0 dp1.2 l=2.8 w=2.0
j171 1 145 145 0 dp1.2 l=2.8 w=2.0
j172 1 133 133 0 dp1.2 l=2.8 w=2.0
j173 1 146 146 0 dp1.2 l=2.8 w=2.0
j174 1 134 134 0 dp1.2 l=2.8 w=2.0
j175 1 147 147 0 dp1.2 l=2.8 w=2.0
j176 1 138 138 0 dp1.2 l=2.8 w=2.0
j177 1 148 148 0 dp1.2 l=2.8 w=2.0
j178 1 141 141 0 dp1.2 l=2.8 w=2.0
j179 1 149 149 0 dp1.2 l=2.8 w=2.0
j180 1 143 143 0 dp1.2 l=2.8 w=2.0
j181 1 150 150 0 dp1.2 l=2.8 w=2.0
j182 151 152 153 0 dp1.1 l=0.8 w=2.0
j183 123 144 0 0 enh.1 l=0.8 w=8.0
j184 144 153 0 0 enh.1 l=0.8 w=8.0
j185 154 152 155 0 dp1.1 l=0.8 w=2.0
j186 127 145 0 0 enh.1 l=0.8 w=8.0
j187 145 155 0 0 enh.1 l=0.8 w=8.0
j188 156 152 157 0 dp1.1 l=0.8 w=2.0
j189 133 146 0 0 enh.1 l=0.8 w=8.0
j190 146 157 0 0 enh.1 l=0.8 w=8.0
j191 158 152 159 0 dp1.1 l=0.8 w=2.0
j192 134 147 0 0 enh.1 l=0.8 w=8.0
j193 147 159 0 0 enh.1 l=0.8 w=8.0
j194 160 152 161 0 dp1.1 l=0.8 w=2.0
j195 138 148 0 0 enh.1 l=0.8 w=8.0
j196 148 161 0 0 enh.1 l=0.8 w=8.0
j197 162 152 163 0 dp1.1 l=0.8 w=2.0
j198 141 149 0 0 enh.1 l=0.8 w=8.0
j199 149 163 0 0 enh.1 l=0.8 w=8.0
j200 164 152 165 0 dp1.1 l=0.8 w=2.0
j201 143 150 0 0 enh.1 l=0.8 w=8.0
j202 150 165 0 0 enh.1 l=0.8 w=8.0
j203 1 152 166 0 dp1.1 l=0.8 w=2.0
j204 1 167 151 0 dp1.1 l=0.8 w=2.0
j205 1 152 168 0 dp1.1 l=0.8 w=2.0
j206 1 167 154 0 dp1.1 l=0.8 w=2.0
j207 1 152 169 0 dp1.1 l=0.8 w=2.0
j208 1 167 156 0 dp1.1 l=0.8 w=2.0
j209 1 152 170 0 dp1.1 l=0.8 w=2.0
j210 1 167 158 0 dp1.1 l=0.8 w=2.0
j211 1 152 171 0 dp1.1 l=0.8 w=2.0
j212 1 167 160 0 dp1.1 l=0.8 w=2.0
j213 1 152 172 0 dp1.1 l=0.8 w=2.0
j214 1 167 162 0 dp1.1 l=0.8 w=2.0
j215 1 152 173 0 dp1.1 l=0.8 w=2.0
j216 1 167 164 0 dp1.1 l=0.8 w=2.0
j217 174 152 175 0 dp1.1 l=0.8 w=2.0
j218 166 167 176 0 dp1.1 l=0.8 w=2.0
j219 177 167 166 0 dp1.1 l=0.8 w=2.0
j220 151 152 178 0 dp1.1 l=0.8 w=2.0
j221 179 152 151 0 dp1.1 l=0.8 w=2.0
j222 168 167 180 0 dp1.1 l=0.8 w=2.0
j223 181 167 168 0 dp1.1 l=0.8 w=2.0
j224 154 152 182 0 dp1.1 l=0.8 w=2.0
j225 0 0 166 0 enh.2 l=7.2 w=7.2
j226 176 174 0 0 enh.1 l=0.8 w=6.0
j227 177 183 0 0 enh.1 l=0.8 w=2.0
j228 0 0 151 0 enh.2 l=9.2 w=9.2
j229 184 152 154 0 dp1.1 l=0.8 w=2.0
j230 169 167 185 0 dp1.1 l=0.8 w=2.0
j231 186 167 169 0 dp1.1 l=0.8 w=2.0
j232 156 152 187 0 dp1.1 l=0.8 w=2.0
j233 178 177 0 0 enh.1 l=0.8 w=6.0
j234 0 0 168 0 enh.2 l=7.2 w=7.2
j235 180 179 0 0 enh.1 l=0.8 w=6.0
j236 181 183 0 0 enh.1 l=0.8 w=2.0
j237 0 0 154 0 enh.2 l=9.2 w=9.2
j238 188 152 156 0 dp1.1 l=0.8 w=2.0
j239 170 167 189 0 dp1.1 l=0.8 w=2.0
j240 190 167 170 0 dp1.1 l=0.8 w=2.0
j241 158 152 191 0 dp1.1 l=0.8 w=2.0
j242 182 181 0 0 enh.1 l=0.8 w=6.0
j243 0 0 169 0 enh.2 l=7.2 w=7.2
j244 185 184 0 0 enh.1 l=0.8 w=6.0
j245 186 183 0 0 enh.1 l=0.8 w=2.0
j246 0 0 156 0 enh.2 l=9.2 w=9.2
j247 192 152 158 0 dp1.1 l=0.8 w=2.0
j248 171 167 193 0 dp1.1 l=0.8 w=2.0
j249 194 167 171 0 dp1.1 l=0.8 w=2.0
j250 160 152 195 0 dp1.1 l=0.8 w=2.0
j251 187 186 0 0 enh.1 l=0.8 w=6.0
j252 0 0 170 0 enh.2 l=7.2 w=7.2
j253 189 188 0 0 enh.1 l=0.8 w=6.0
j254 190 183 0 0 enh.1 l=0.8 w=2.0
j255 0 0 158 0 enh.2 l=9.2 w=9.2
j256 196 152 160 0 dp1.1 l=0.8 w=2.0
j257 172 167 197 0 dp1.1 l=0.8 w=2.0
j258 198 167 172 0 dp1.1 l=0.8 w=2.0
j259 162 152 199 0 dp1.1 l=0.8 w=2.0
j260 191 190 0 0 enh.1 l=0.8 w=6.0
j261 0 0 171 0 enh.2 l=7.2 w=7.2
j262 193 192 0 0 enh.1 l=0.8 w=6.0
j263 194 183 0 0 enh.1 l=0.8 w=2.0
j264 0 0 160 0 enh.2 l=9.2 w=9.2
j265 200 152 162 0 dp1.1 l=0.8 w=2.0
j266 173 167 201 0 dp1.1 l=0.8 w=2.0
j267 202 167 173 0 dp1.1 l=0.8 w=2.0
j268 164 152 203 0 dp1.1 l=0.8 w=2.0
j269 195 194 0 0 enh.1 l=0.8 w=6.0
j270 0 0 172 0 enh.2 l=7.2 w=7.2
j271 197 196 0 0 enh.1 l=0.8 w=6.0
j272 198 183 0 0 enh.1 l=0.8 w=2.0
j273 0 0 162 0 enh.2 l=9.2 w=9.2
j274 199 198 0 0 enh.1 l=0.8 w=6.0
j275 0 0 173 0 enh.2 l=7.2 w=7.2
j276 201 200 0 0 enh.1 l=0.8 w=6.0
j277 202 183 0 0 enh.1 l=0.8 w=2.0
j278 0 0 164 0 enh.2 l=9.2 w=9.2
j279 203 202 0 0 enh.1 l=0.8 w=6.0
j280 1 167 204 0 dp1.1 l=0.8 w=2.0
j281 204 152 205 0 dp1.1 l=0.8 w=2.0
j282 1 183 183 0 dp1.2 l=1.6 w=2.0
j283 1 152 206 0 dp1.1 l=0.8 w=2.0
j284 206 167 207 0 dp1.1 l=0.8 w=2.0
j285 1 167 208 0 dp1.1 l=0.8 w=2.0
j286 205 209 0 0 enh.1 l=0.8 w=6.0
j287 206 167 209 0 dp1.1 l=0.8 w=2.0
j288 204 152 210 0 dp1.1 l=0.8 w=2.0
j289 183 210 0 0 enh.1 l=0.8 w=16.0
j290 204 0 0 0 enh.2 l=7.2 w=7.2
j291 0 211 205 0 enh.1 l=0.8 w=6.0
j292 207 212 0 0 enh.1 l=0.8 w=6.0
j293 208 152 213 0 dp1.1 l=0.8 w=2.0
j294 151 152 212 0 dp1.1 l=0.8 w=2.0
j295 214 167 211 0 dp1.1 l=0.8 w=2.0
j296 206 0 0 0 enh.2 l=9.2 w=9.2
j297 0 215 207 0 enh.1 l=0.8 w=6.0
j298 1 152 216 0 dp1.1 l=0.8 w=2.0
j299 216 167 217 0 dp1.1 l=0.8 w=2.0
j300 216 167 218 0 dp1.1 l=0.8 w=2.0
j301 1 167 219 0 dp1.1 l=0.8 w=2.0
j302 217 220 0 0 enh.1 l=0.8 w=6.0
j303 219 152 221 0 dp1.1 l=0.8 w=2.0
j304 154 152 220 0 dp1.1 l=0.8 w=2.0
j305 219 152 215 0 dp1.1 l=0.8 w=2.0
j306 207 222 0 0 enh.1 l=0.8 w=6.0
j307 208 152 222 0 dp1.1 l=0.8 w=2.0
j308 0 218 213 0 enh.1 l=0.8 w=6.0
j309 208 0 0 0 enh.2 l=7.2 w=7.2
j310 216 0 0 0 enh.2 l=9.2 w=9.2
j311 0 223 217 0 enh.1 l=0.8 w=6.0
j312 1 152 224 0 dp1.1 l=0.8 w=2.0
j313 224 167 225 0 dp1.1 l=0.8 w=2.0
j314 224 167 226 0 dp1.1 l=0.8 w=2.0
j315 225 227 0 0 enh.1 l=0.8 w=6.0
```

```
j316 160 152 227 0 dp1.1 l=0.8 w=2.0
j317 156 152 223 0 dp1.1 l=0.8 w=2.0
j318 217 228 0 0 enh.1 l=0.8 w=6.0
j319 151 152 228 0 dp1.1 l=0.8 w=2.0
j320 0 226 221 0 enh.1 l=0.8 w=6.0
j321 219 0 0 0 enh.2 l=7.2 w=7.2
j322 224 0 0 0 enh.2 l=9.2 w=9.2
j323 0 229 225 0 enh.1 l=0.8 w=6.0
j324 162 152 229 0 dp1.1 l=0.8 w=2.0
j325 225 230 0 0 enh.1 l=0.8 w=6.0
j326 158 152 230 0 dp1.1 l=0.8 w=2.0
j327 0 0 231 0 enh.2 l=7.2 w=7.2
j328 232 233 0 0 enh.1 l=0.8 w=7.2
j329 0 234 235 0 enh.1 l=0.8 w=4.0
j330 175 0 0 0 enh.2 l=7.2 w=7.2
j331 236 152 233 0 dp1.1 l=0.8 w=2.0
j332 0 0 237 0 enh.2 l=7.2 w=7.2
j333 238 239 0 0 enh.1 l=0.8 w=7.2
j334 0 240 241 0 enh.1 l=0.8 w=7.2
j335 242 152 240 0 dp1.1 l=0.8 w=2.0
j336 232 167 243 0 dp1.1 l=0.8 w=8.0
j337 241 167 244 0 dp1.1 l=0.8 w=8.0
j338 235 152 175 0 dp1.1 l=0.8 w=2.0
j339 231 167 234 0 dp1.1 l=0.8 w=2.0
j340 244 243 231 0 enh.1 l=0.8 w=8.0
j341 243 244 231 0 enh.1 l=0.8 w=8.0
j342 175 167 1 0 dp1.1 l=0.8 w=2.0
j343 0 245 246 0 enh.1 l=0.8 w=4.0
j344 236 0 0 0 enh.2 l=7.2 w=7.2
j345 158 152 239 0 dp1.1 l=0.8 w=2.0
j346 0 247 248 0 enh.1 l=0.8 w=7.2
j347 160 152 247 0 dp1.1 l=0.8 w=2.0
j348 238 167 249 0 dp1.1 l=0.8 w=8.0
j349 248 167 250 0 dp1.1 l=0.8 w=8.0
j350 231 152 1 0 dp1.1 l=0.8 w=2.0
j351 244 152 1 0 dp1.1 l=0.8 w=2.0
j352 243 152 1 0 dp1.1 l=0.8 w=2.0
j353 246 152 236 0 dp1.1 l=0.8 w=2.0
j354 237 167 245 0 dp1.1 l=0.8 w=2.0
j355 250 249 237 0 enh.1 l=0.8 w=8.0
j356 249 250 237 0 enh.1 l=0.8 w=8.0
j357 236 167 1 0 dp1.1 l=0.8 w=2.0
j358 1 251 252 0 enh.1 l=0.8 w=6.0
j359 251 152 253 0 dp1.1 l=0.8 w=2.0
j360 237 152 1 0 dp1.1 l=0.8 w=2.0
j361 250 152 1 0 dp1.1 l=0.8 w=2.0
j362 249 152 1 0 dp1.1 l=0.8 w=2.0
j363 1 254 255 0 dp1.1 l=0.8 w=10.0
j364 1 152 256 0 dp1.1 l=0.8 w=2.0
j365 1 167 242 0 dp1.1 l=0.8 w=2.0
j366 257 152 258 0 dp1.1 l=0.8 w=2.0
j367 256 167 259 0 dp1.1 l=0.8 w=2.0
j368 260 167 256 0 dp1.1 l=0.8 w=2.0
j369 242 152 261 0 dp1.1 l=0.8 w=2.0
j370 252 167 214 0 dp1.1 l=0.8 w=2.0
j371 0 0 256 0 enh.2 l=7.2 w=7.2
j372 259 257 0 0 enh.1 l=0.8 w=6.0
j373 214 152 0 0 dp1.1 l=0.8 w=2.0
j374 214 0 0 0 enh.2 l=7.2 w=7.2
j375 0 0 242 0 enh.2 l=9.2 w=9.2
j376 262 255 262 0 dp1.3 l=2.0 w=4.0
j377 152 262 152 0 dp1.3 l=2.0 w=4.0
j378 261 260 0 0 enh.1 l=0.8 w=6.0
j379 152 263 263 0 dp1.1 l=0.8 w=2.0
j380 263 263 167 0 dp1.1 l=0.8 w=2.0
j381 264 265 264 0 dp1.3 l=2.0 w=4.0
j382 167 264 167 0 dp1.3 l=2.0 w=4.0
j383 0 266 267 0 enh.1 l=0.8 w=16.0
j384 0 268 266 0 enh.1 l=0.8 w=16.0
j385 0 269 268 0 enh.1 l=0.8 w=16.0
j386 0 267 254 0 enh.1 l=0.8 w=16.0
j387 0 267 270 0 enh.1 l=0.8 w=16.0
j388 267 267 1 0 dp1.2 l=1.6 w=2.0
j389 266 266 1 0 dp1.2 l=1.6 w=2.0
j390 268 268 1 0 dp1.2 l=1.6 w=2.0
j391 0 271 269 0 enh.1 l=0.8 w=16.0
j392 254 270 1 0 enh.1 l=0.8 w=16.0
j393 270 270 1 0 dp1.2 l=1.6 w=2.0
j394 269 269 1 0 dp1.2 l=1.6 w=2.0
j395 269 272 0 0 enh.1 l=0.8 w=16.0
j396 1 273 274 0 enh.1 l=0.8 w=16.0
j397 1 273 273 0 dp1.2 l=1.6 w=2.0
j398 1 275 275 0 dp1.2 l=1.6 w=2.0
j399 1 272 272 0 dp1.2 l=1.6 w=2.0
j400 1 276 276 0 dp1.2 l=1.6 w=2.0
j401 0 266 277 0 enh.1 l=0.8 w=16.0
j402 1 271 271 0 dp1.2 l=1.6 w=2.0
j403 277 277 1 0 dp1.2 l=1.6 w=2.0
j404 274 275 0 0 enh.1 l=0.8 w=16.0
j405 273 275 0 0 enh.1 l=0.8 w=16.0
j406 275 272 0 0 enh.1 l=0.8 w=16.0
j407 272 276 0 0 enh.1 l=0.8 w=16.0
j408 276 277 0 0 enh.1 l=0.8 w=16.0
j409 277 278 0 0 enh.1 l=0.8 w=16.0
j410 271 278 0 0 enh.1 l=0.8 w=16.0
j411 265 274 1 0 dp1.1 l=0.8 w=10.0
j412 108 279 253 0 enh.1 l=0.8 w=16.0
j413 108 279 279 0 dp1.2 l=1.6 w=2.0
j414 108 280 281 0 enh.1 l=0.8 w=16.0
j415 108 282 282 0 dp1.2 l=1.6 w=2.0
j416 108 283 283 0 dp1.2 l=1.6 w=2.0
j417 108 284 285 0 enh.1 l=0.8 w=16.0
j418 253 282 101 0 enh.1 l=0.8 w=16.0
j419 279 282 101 0 enh.1 l=0.8 w=16.0
j420 281 101 101 0 dp1.2 l=1.6 w=2.0
j421 108 286 286 0 dp1.2 l=1.6 w=2.0
j422 108 286 278 0 enh.1 l=0.8 w=16.0
j423 108 287 258 0 enh.1 l=0.8 w=16.0
j424 108 287 287 0 dp1.2 l=1.6 w=2.0
j425 108 288 289 0 enh.1 l=0.8 w=16.0
j426 283 285 101 0 enh.1 l=0.8 w=16.0
j427 282 281 101 0 enh.1 l=0.8 w=16.0
j428 285 101 101 0 dp1.2 l=1.6 w=2.0
j429 108 290 290 0 dp1.2 l=1.6 w=2.0
j430 286 283 101 0 enh.1 l=0.8 w=16.0
j431 278 283 101 0 enh.1 l=0.8 w=16.0
j432 258 290 101 0 enh.1 l=0.8 w=16.0
j433 287 290 101 0 enh.1 l=0.8 w=16.0
j434 289 101 101 0 dp1.2 l=1.6 w=2.0
j435 290 289 101 0 enh.1 l=0.8 w=16.0
j436 108 280 108 0 dp1.3 l=2.0 w=50.0
j437 108 284 108 0 dp1.3 l=2.0 w=50.0
j438 108 288 108 0 dp1.3 l=2.0 w=50.0
j439 108 280 108 0 dp1.3 l=2.0 w=50.0
j440 108 284 108 0 dp1.3 l=2.0 w=50.0
j441 108 288 108 0 dp1.3 l=2.0 w=50.0
j442 280 101 280 0 dp1.3 l=2.0 w=50.0
j443 284 101 284 0 dp1.3 l=2.0 w=50.0
j444 288 101 288 0 dp1.3 l=2.0 w=50.0
j445 280 101 280 0 dp1.3 l=2.0 w=50.0
j446 284 101 284 0 dp1.3 l=2.0 w=50.0
j447 288 101 288 0 dp1.3 l=2.0 w=50.0

*analysis parameters
.options scale=1E-06 post
.tran 10ps 45000ps
.MEAS avg_power avg power
.MEAS max_power max power
.MEAS rms_power rms power
.MEAS TRAN Avg_P_VDD AVG P(Vdd) FROM=0.0ns TO=20ns
.MEAS TRAN Avg_P_VSS AVG P(Vss) FROM=0.0ns TO=20ns
.end
```

APPENDIX E. C++ CODE FOR TOTAL GATE AREA CALCULATION

```
/* Gate-area.cpp
**
** Program computes the total gate area of a
** given HSpice file
*/

#include <fstream.h>;
#include <cstring.h>;
#include <math.h>;

int main(int argc, char *argv[])
{
  ifstream f_HSpice(argv[1]);   // Instantiate an input stream
  string text_line,len_str,wid_str;
  double len_flt,wid_flt,tot_area=0.0;
  size_t len_beg,len_end,wid_beg,wid_end;

  if (f_HSpice){
       while (!f_HSpice.eof()){
             text_line.read_line(f_HSpice);

             if (text_line.contains("l=")) {
                  len_beg = text_line.find("l=")+2;
                  len_end = text_line.find(".",len_beg)+2;
                  len_str = text_line.substr(len_beg,len_end-len_beg);
                  len_flt = atof(len_str.c_str());

                  wid_beg = text_line.find("w=")+2;
                  wid_end = text_line.find(".",wid_beg)+2;
                  wid_str = text_line.substr(wid_beg,wid_end-wid_beg);
                  wid_flt = atof(wid_str.c_str());

                  tot_area+=len_flt*wid_flt;
             }
       }
       cout<<"The total gate area is "<<tot_area;
       return 1;
  }
  else {
       cout<<"Unable to open file "<<argv[1]<<".";
       return 0;
  }
}
```

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